AFWAL-TR-82-206 **VOLUME II**

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ADVANCED ULTRA-VIOLET (UV) AIRCRAFT FIRE DETECTION SYSTEM **VOLUME II - SYSTEM HARDWARE DESIGN,** SOFTWARE DESIGN, AND TEST



GENERAL DYNAMICS/FORT WORTH DIVISION P.O. BOX 748 FORT WORTH, TEXAS 76101

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FINAL REPORT FOR PERIOD DECEMBER 1977 - OCTOBER 1981

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This technical report has been reviewed and is approved for publication.

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18. SUPPLEMENTARY NOTES

This report consists of 3 volumes.

Volume I - System Description and Flight Test

Volume III - Ground Support Equipment (GSE) For System Checkout

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Vltra-Violet Fire Detection Microprocessor Engine Nacelle

The objective of this program was to utilize ultra-violet (UV) radiation technology to provide advanced means of detecting fire hazards more reliably and more rapidly than current thermally activated continuous cable type system. This volume, Volume II, of three volumes provides detail information on the development, circuit/software design and qualification testing of the system component.

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The work reported herein was performed in accordance with Air Force Contract F33615-77-C-2029 under the direction of the Fire Protection Branch (AFWAL/POSH) of the Fuels and Lubrication Division, Aero Propulsion Laboratory, Air Force Wright Aeronautical Laboratories, Wright-Patterson Air Force Base, Ohio, under Project 2348, Task 01, Work Unit 02, with Mr G.T. Beery and Mr T.A. Hogan, AFWAL/POSH, as Project Engineers.

This report is the result of utilizing ultra-violet (UV) radiation technology in the development and flight testing of an advanced aircraft fire detection system.

The contractor was General Dynamics, Fort Worth Division, Fort Worth, Texas. Mr. R.J. Springer, Program Manager, directed the efforts of P.H. Lang, W.B. Kirk, B.B. Witte, D.C. Nelson, and J. Phillips. The overall effort was under the supervision of Mr. C.E. Porcher, Manager, Propulsion and Thermodynamics Section. Graviner Ltd./HTL Industries, General Dynamics subcontractor, accomplished the design, fabrication, environmental testing and support for the flight test phase of the program. Graviner/HTL's efforts were directed by Mr. S.P. Robinson who was supported by P.H. Sheath and D.J.V. Smith. Sacramento Air Logistics Command (SM-ALC) provided the F-111 aircraft and support for the flight test phase of the program. Mr B.W. Nichols, SM-ALC Engineering, coordinated the flight testing at McClellan Air Force Base.

This report describes the results of work conducted during the period of 15 December 1977 to 26 October 1981.

This is Volume II of three volumes. Volume I describes the overall work of the program which includes the results of the flight test phase. Volume II contains a description and details of the system circuit and software design. Volume III contains a description and details of the Ground Support Equipment (GSE) which is used as a fault diagnostic maintenance tool.

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SUMMARY

Analysis and details that include the electrical circuit, power supply, microprocessor boards, and logic cards were completed for each component in the system. In addition a software program was completed that included initialization, processing of adjacency and absent head information, software assembly listings, instruction summaries for the RCA 1802 microprocessor, and the COSMAC Level 2 assembly language of the microprocessor. A qualification test was completed after the design and fabrication of the system components.

1.0 INTRODUCTION

1.1 Microprocessor Selection

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The trade study determined that the design should be based on the use of a microprocessor. Microprocessor evaluations determined that the RCA 1802 microprocessor would best provide the needs of the system requirements. The CMOS design, low power consumption, and low immunity to noise were the primary features for the selection of the 1802 for the UV fire detection system.

1.2 Microprocessor Integration

The integration of the microprocessor into the system design provides the flexibility and programmability needed to meet the high reliability requirements of this program.

2.0 COMPONENT DESIGN

2.1 Detectors

The main design constraints of the sensor heads arose from the requirement to use the proven Graviner D6100 UV cell with its associated UV test emitter, to withstand the environmental conditions of a military aircraft engine installation and to be as small and lightweight as possible. Physical characteristics are shown on Figures 2-1,2-2 and on Installation Schematics Figures 2-3 and 2-4.

Within these design constraints the configurations developed and shown on drawings 53522-011 and 53521-012 are probably close to and optimum. (References 2-1 and 2-2.)

The designs are based on the assumption of production quantities that would justify expenditure on tooling for pressed steel casework but the sensor assemblies used during this program were fabricated without tooling to simulate the proposed production design.

The photocell and protective quartz dome are mounted on a thin steel retainer with a fillet of silicone potting compound. This assembly is then spot welded to the case. In early development samples, some difficulties were experienced with emitter glass envelopes cracking during low temperature tests but this was later overcome by incorporating a resilient rubber compound coating prior to emitter assembly.

The simple mounting base is intended for use with a variety of aircraft brackets which might be necessary to provide appropriate viewing directions in an engine installation.

The assembly meets the required life of 10,000 hours at 250°C with the exception of the electrical connector, which has a life limited by the manufacture to 1000 hours at 250°C.

2.2 Component Design - Computer Control Unit

2.2.1 Construction

System A and System B electronic circuitry is contained in mechanically identical racking. General Assembly drawings 53813-203 and 53813-204 show pictorially the systems'-contruction. (References 2-3 and 2-4.) Physical characteristics are shown on Figure 2-5.

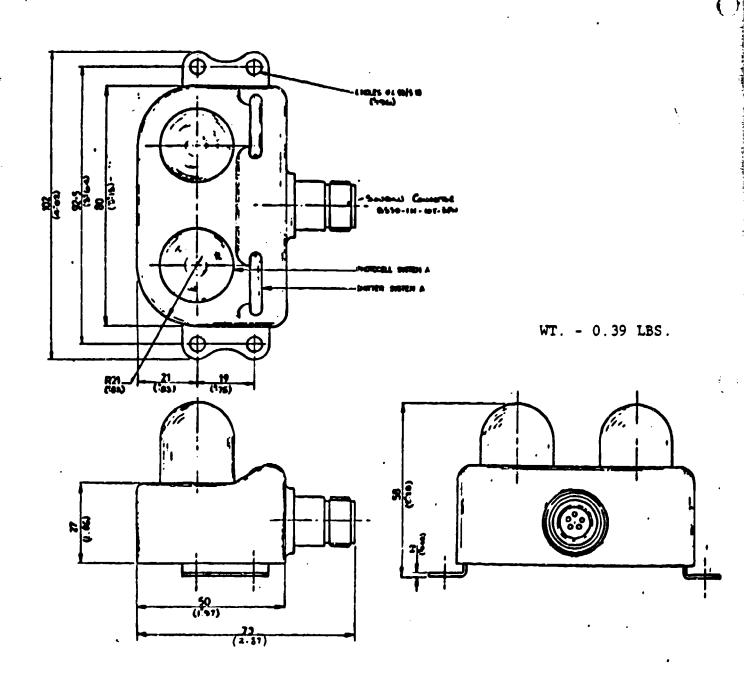
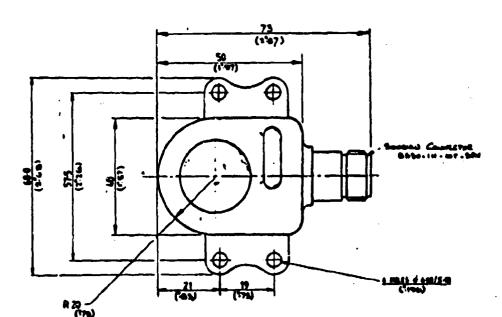
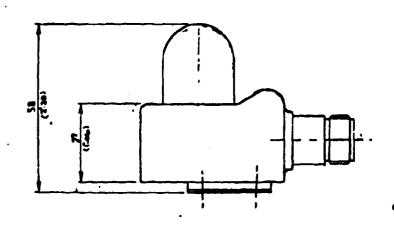


FIGURE 2-1 UV DETECTOR DUAL HEAD



WT. - 0.22 LBS



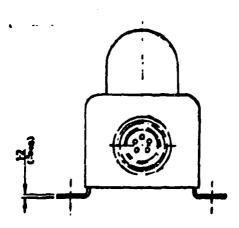


FIGURE 2-2 UV DETECTOF SINGLE HEAD 5

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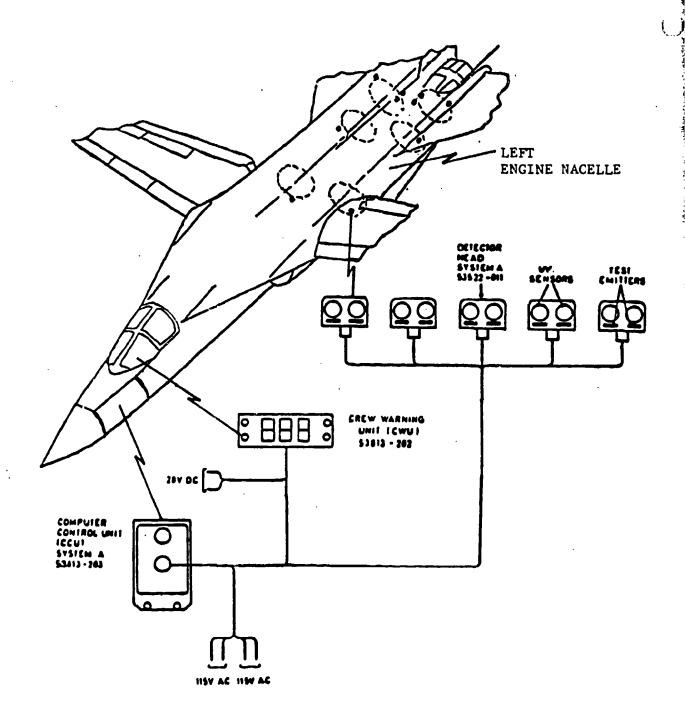


FIGURE 2-3 SYSTEM 'A' INSTALLATION SCHEMATIC

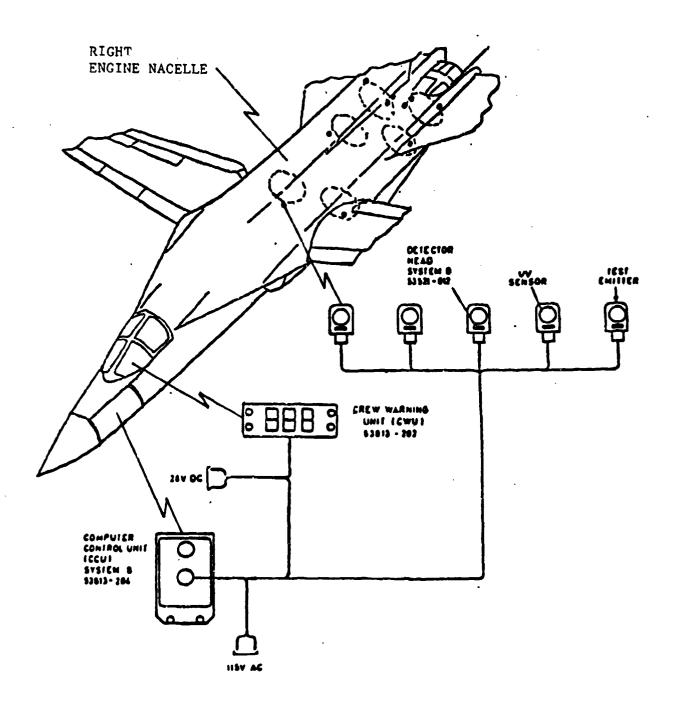


FIGURE 2-4 SYSTEM 'B' INSTALLATION SCHEMATIC

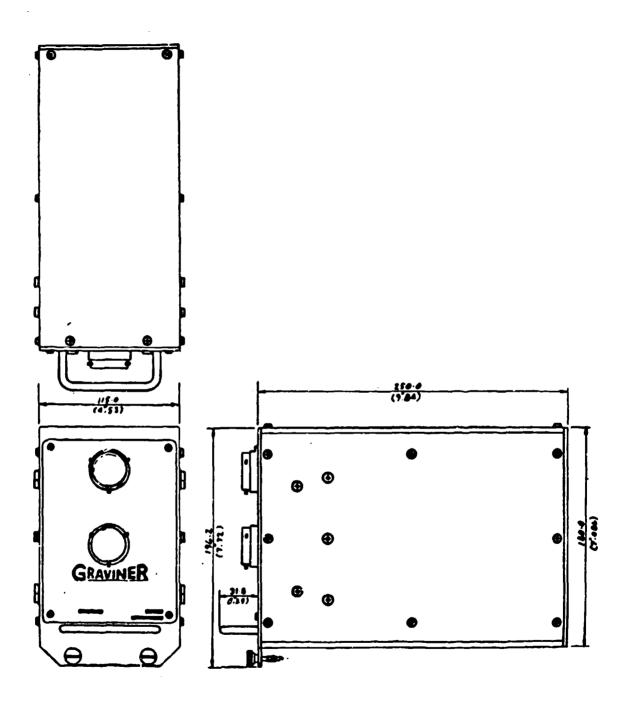


FIGURE 2-5 COMPUTER CONTROL UNIT

The essential features of both systems are as follows:

a) It is a box construction consisting of formed top, bottom and side panels, with two similar cast end plates. The rear panel has on its external face indented locating slots to ensure correct positioning of the units in the aircraft racking and on its internal face it contains guides to ensure location and adequate fixing for the printed circuit boards.

The front panel has mounted through it, two captive knurl headed screws to provide fixing to the aircraft racking. Two circular electrical multipin connectors are mounted through the front panel. One, termed on the front panel label the 'aircraft plug', routes to the electronics power and signals from detectors and also carries the signals to the crew warning unit (CWU). The second connector, termed the GSE plug, is utilized when the system is interrogated by ground support equipment and is not normally used when the aircraft is operational.

Internally, the box contains a cross member which acts to make the construction more rigid. To this are attached the printed circuit board guides,

- b) Within the box a mother board printed circuit card acts to connect the various parts of the control unit electronics together. On the mother board are mounted connectors which mate with the cable harness connected to the two circular connectors, and to the daughter board connectors. The mother board also houses the transformer for the systems' power supply requirements.
- c) A filter board is mounted on the front panel, close to the aircraft plug such that incoming power can be filtered.
- d) The printed circuit cards contained within the units are interconnected via the mother board, and consist of, in the case of System A, a common logic card, two microprocessor cards, two head drive cards, a master logic card and a slave logic card. In the case of System B, the unit contains a common logic card, a microprocessor card, a head drive card, a master logic card and a battery card which is braced such that the mass of batteries does not cause vibration problems. Each card edge connector is polarized such that boards cannot be incorrectly located within the boxes.

84.

2.2.2 Circuit Description

A block diagram of the CCU is shown in Figure 2-6. This is shown to give a general appreciation of the way the CCU printed boards interface with each other. Circuit description is essentially on a board by board basis. Reference is made to the CCU circuit diagram 53813-203CD (System A) or 53813-204CD (System B), for a clearer understanding of the way cards are interconnected. (References 2-5 and 2-6.)

2.2.2.1. Drive Supply Card

(Circuit diagram 43761-143-CD) - Reference 2-7

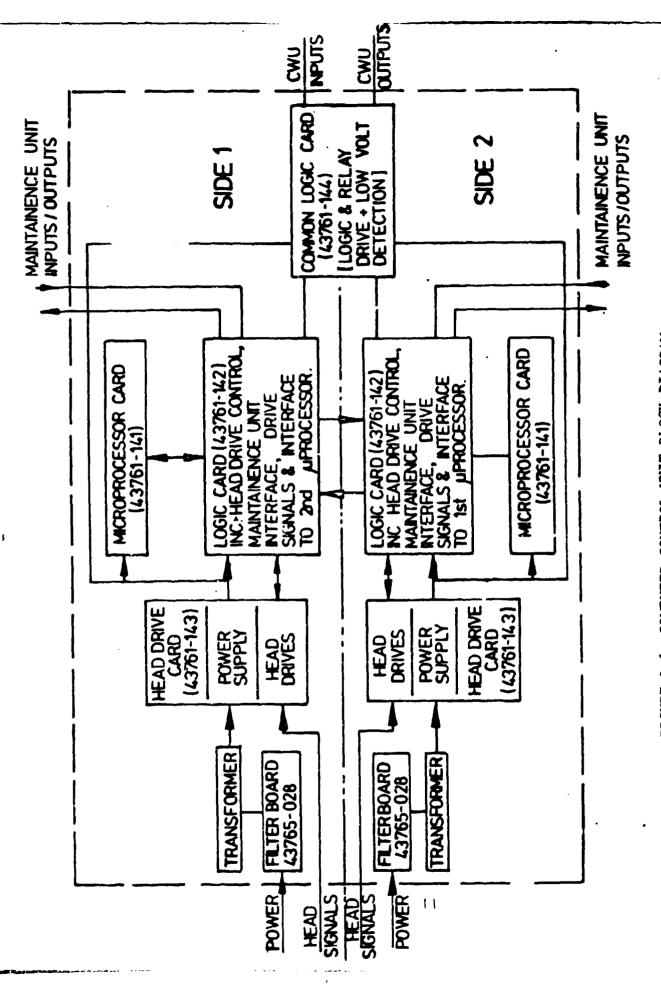
The drive supply card consists of a 320v DC stabilized supply, a 5.6v and a 5v DC stabilized supply, 8 head drive circuits, an emitter drive circuit and a low voltage detection reference.

2.2.2.1.1. 320v DC Supply

The AC voltage from the transformer's secondary winding No.1 is rectified via the bridge rectifier D1, D2, D3 and D4 and smoothed by C1. C31 is a radio frequency suppression capacitor. This voltage is then stabilized to 320v DC by means of a series feedback regulator. D12 and R6 provide a reference voltage for the emitter of TR3. R9 and R11 potentially divide the output voltage which feeds the base of TR3. As the cutput voltage increases, TR3 base rises above the reference voltage and TR3 starts to conduct. This in turn clamps the base of TR2 and the output voltage. D16 protects TR2 from exceeding its reverse voltage rating. The base drive to TR2 is provided by a constant current source generated by TR1. D9 and R1 set up a reference voltage for the base of TR1. R4 sets up a constant current in the emitter lead of TR1. Hence a constant current is developed in the collector of TR1. The 320v DC supply powers the head drive circuits and the emitter drive circuits.

2.2.2.1.2. 5.6v and 5v DC Supply

The AC voltage from the transformer's secondary winding No. 2 is rectified via the bridge rectifier D5, D6, D7 and D8 and smoothed by C3. C2 is a radio frequency suppression capacitor. This voltage is then stabilized to 5.6v via an emitter follower regulator. A reference voltage at the base junction of TR4 is set up by R7 and the combined forward voltages of D13, D14 and D15. R8 sets up a constant current in the emitter lead of TR4. This in turn sets up a constant current in the collector lead which supplies zener diode, D17, and base drive to TR5. D17 provides a reference voltage (6.2v) at the base junction of TR5 causing the emitter of TR5 to provide a 5.6 volt output. C4 smooths this voltage and acts as an energy store for sudden surges in current. D18 protects TR5 base emitter junction from exceeding its reverse voltage rating when supply is switched off.



4 . 4 b

7

FIGURE 2-6 COMPUTER CONTROL UNIT BLOCK DIAGRAM

Two further supplies are generated from this voltage via D19 and D20. The 5.6v supplies power to the common output logic card. The 5.6v supply via D20 powers all logic and microprocessor devices except the RAM which is powered via D19. This ensures that the RAM is isolated in the event of supply failure or disconnection. In this case the RAM is powered by a separate battery pack as detailed in Section 2.2.2.6.

2.2.2.1.3. Low Voltage Detection

This circuit monitors the rectifier voltage of the transformers No. 2 secondary winding. The voltage is potentially divided by plo,R2,R3 and R71. The voltage across R3 is fed to the common logic card. This circuit provides an early warning signal to the microprocessor that the supply is fa ling as detailed in Section 2.2.2.4.4.2.

2.2.2.1.4.. Head Drive Circuit

The head drive circuit is designed to enable one side of the photocell to be common with the Ov line. Thereby, minimizing the amount of wiring required in the aircraft and control unit. The head circuit consists of four sections:

- i) The Detector Current Sensor,
- ii) Head Turn Off Time Control Circuit. (not part of the drive supply card)
- iii) Head Turn Off
 - iv) Current Limit Circuit

Circuit description relates to head drive 1 consisting of transistors TR6, 7 and 14 with associated components.

2.2.2.1.4.1. The Detector Current Sensor

The head current sensor PNP transistor TR14, which in standby mode is biased off. When the supply is switched on the capacitance across the leads to the photocell charges up via R32. R72 and C23 are designed to charge up at a slower rate than R32, R and the lead capacitance therefore reverse biasing the base emitter junctions of TR14 and holding it off. D38 protects the base emitter junction of TR14 from exceeding its reverse voltage rating.

when UV is present at the photocell it will conduct causing current to be drawn through R, R32, R72 and the emitter base junction of TR14. TR14 conducts and current flows through R24 and R25. C5 reduces the radio frequency interference generated when the current sensor circuit is operating. The voltage across R25 is coupled via C9 to the head turn off timing control circuit on the logic card.

2.2.2.1.4.2. Head Turn off Time Control Circuit

The head turn off timing circuit is described in Section 2.2.2.3.5.

2.2.2.1.4.3. Head Turn Off

The output from the logic card feeds the base junction of TR7. R13 is a pull down resistor to ensure TR7 does not turn itself ON due to collector base leakage current. A 5 volt signal from the logic card causes TR7 to turn ON. The potential divider chain, R12 R20 then clamps the base of TR6 to approximately 15v. TR6 acts as an emmitter follower, therefore the voltage across the photocell is reduced to approximately 15v allowing the photocell to deionize. At the end of the timing period the signal from the logic card returns to 0v. TR7 turns off allowing TR6 to be turned on by R12 returning the photocell voltage to 320v.

2.2.2.1.4.4. Current Limit Circuit

If the head lead becomes short circuit to ground, TR14 turns hard ON and an output pulse is passed to the logic card. TR7 turns on and the voltage across the photocell drops to approximately 15v. At the end of the head time off period TR7 turns off allowing TR6 to turn on, but as TR14 is being held hard on excessive current is being drawn through R80. When the voltage developed across the base emitter junction of TR6 and R80 equals the combined forward voltages of D25 and D55 no further increase in TR6 base drive occurs, and hence the current is limited. D47 isolates the head circuit from seeing negative going spikes.

2.2.2.1.5. Emitter Drive Circuit

The emitter drive circuit is designed so that a maximum of 8 emitters can be powered at one time. The emitters are connected in parallel to minimize aircraft and control unit wiring. The circuit consists of three parts:

- i) Time Sharing 350v Switch.
- ii) Emiter Enable Circuit (Head Test)
- iii) Emitter Verify Circuit.

2.2.2.1.5.1. Time Sharing 350v Switch

The voltage to the emitter enable circuit is controlled by the time share switch. The timeshare signal from the logic card (at pin 8) is a square wave. When the output is high TR30 turns on via a base current limiting resistor R4 (on logic card), this holds TR32 off. TR31 is turned on by R62 and 350v DC is supplied to the emitter enable circuit. When the output of the logic card goes low, TR30 turns off and TR32 turns ON via R61 pull up resistor.R62 and R63 potentially divides the 350v supply clamping the base of TR31 to approximately 154v. The emitters, which require greater then 90v to strike, will therefore turn off. R60 is a pull down leakage current resistor for TR30 emitter base junction.

2.2.2.1.5.2. Emitter Enable Circuit

Under standby condition i.e. emitter off, the head test input (pin 9) from the logic card is low (0v). TR34 is, therefore, turned ON via R65 pull up resistor. R64 and R66 potentially divide the voltage from the time share switch which clamps the base of TR33 to approximately 25v when TR21 emitter voltage is high and approximately lv when it is low. TR33 is an emitter follower and 25v or lv is fed to the emitters (connected at pin 15) via a current limiting resistor R69.

When the head test input goes high, the emitter of TR34 is held at 5v.

Because the pull up resistor R65 is supplied from the 5v power supply, TR34 turns off and TR33 turns on via pull up resistor, R64. The voltage at the emitter TR33 will then follow the voltage at TR31 emitter which changes from 350v to 15v in sympathy with the time share input. D37 protects TR33 from exceeding its reverse voltage rating when it turns off.

2.2.2.1.5.3. Emitter Verify

The circuit monitors the output voltage to the emitters so that the microprocessor can confirm when the emitters are on. The output voltage from TR33 is potentially divided by R67 and R68. The junction of these resistors feeds the base of TR35. When the emitter line voltage is high (350v), there is sufficient voltage at the base of TR35 to turn it ON. The collector of TR35 goes low which feeds the EF3 (NOT) input of the microprocessor card. When the output goes low TR35 turns off and the output is pulled up via R70 to the 5v line. Recause the lead capacitance tends to hold the emitters on for a short period after the emitter circuit has been switched off, it is necessary to discharge this capacitance.

2.2.2.2. Microprocessor Boards

(Circuit diagram reference 43761-141CD) - Reference 2-8

The microprocessor card houses a CMOS microprocessor (IC1) CDP 1802 CD and CMOS memory consisting of 3K bytes of read only memory (ROM) and 256 bytes of random access memory (RAM). All other integrated circuits contained on the card are CMOS to ensure high noise immunity and low power consumption. The ROM consists of 6 IC's, IC5 - IC10 each being UV erasible 512 word 8 bit configured parts, IM 6654MJG, manufactured by Intersil. RAM is formed by IC2 and IC3 configured as 256 bit by 4 manufactured by RCA, part number CDP 1822CD.

Memory is arranged such that ROM resides between locations H'OOOO' and H'OBFF' and RAM resides between locations H'OCOO' and H'OCFF'. This is controlled by IC4 (CDP1859CD) which latches and decodes address line information as further described.

4.5

The microprocessor issues the address on to the data bus in two bytes. Firstly, the upper byte, whose correct presence is defined by a timing pulse TPA whose negative edge is used to latch the address into the 4 bit latch/decoder IC4 via its clock input (CK). At the time immediately after the falling edge of TPA, the address All, AlO, A9 and A8 have been latched into IC4 via address line A3 to AO. The truth table of IC4 shows that A8 and A9 and their compliments are provided as latched outputs while AlO and All are decoded into lof 4 format such that when the true address is present, the appropriate chip enable is driven to a 'O' state. Therefore, the CE (NOT) lines act to select between M'OOOO' and M'O3FF' when CEO (NOT) is true, between M'O4OO' and M'O7FF', when CEI (NOT) is true and between H'O8OO' amd H'OBFF', when CE2 (NOT) is true, i.e. between O and IK byte, 1K byte and 2K bytes or between 2K bytes and 3k bytes.

The latched outputs A9 and A9 (NOT) serve to further decode the address. When the address is in the lower half of the required 1K byte range (i.e. between 0 and 512) then A9 (NOT) is at logic 'l' and A9 is at logic'O'thus selecting from the upper bank of ROM (IC5, IC7, and IC9) since the E2 (NOT) input of the IM 6654 requires a 'O' signal to be selected. The latched A8 line from IC4 is connected to all ROM A8 inputs.

ROM's IM6654 will latch internally on the address lines at the occurrence of a negative going edge on El (NOT) only if the chips Sl (NOT) line is held low. Because of this it is necessary to create a suitable signal to input as an El (NOT) control at a time when all required inputs are available on the address bus.

This is done by delaying the TPA pulse for two system clock cycles and utilizes ICl3 to effect the delay. The crystal (XTAL) output from the microprocessor is used to act as a clock pulse into the first stage divider of ICl3. The data input to this divider is the TPA pulse. Initially, when the system is switched on, both Q outputs of ICl3 are reset, caused by a control signal provided to the reset inputs. At this first occurrence of TPA, a 'l' is clocked through to the output of the first stage of ICl3. A second clock pulse occurring at the clock input transfers this '1' level through to the second stage output which is connected to all ROM El (NOT) inputs. The advent of a third clock pulse causes a negative going edge at El (NOT) required for latching of address lines into the ROM. This occurs approximately 1.5 clock cycles after the negative going edge of TPA has occurred and at a time when the lower order address byte has been issued by the microprocessor and has become stable on

the address bus. If the chip has been selected at the time the El (NOT) line input changes from a 'l' to a 'O' state, then the address lines AO - A8 and chip enable line 22 (NOT) are latched into the ROM causing the selected location to place its contents in the MRD output of the microprocessor such that the ROM cannot be enabled on to the data bus during a memory write cycle. During this time the EN (NOT) line is held high thus disabling the CE (NOT) outputs to a deselected 'l' state.

Address line decoding for the 256 bytes of RAM is effected by the nand gate of IC11 and D type flip flops of IC12 whose Q output is initially set to a'l' switch on by coupling the clear line to the set input of IC12 via an inverting buffer of IC11. Since the address range of the RAM is OCOO to OCFF, the two inputs to the and gate are used to detect the presence of a 'l' level on address lines AlO and All (A3 and A2 during the upper byte address cycle). When both AlO and All are present the output of the nand gate goes to a '0' state. TPA signal is inverted by an invert gate of ICll such that a positive edge will occur at the clock input of ICl2 at the time TPA goes low. The result of which is that the output of the nand gate is latched on to the Q output of IC12 . A 'O' Q output is then used as a chip enable for the RAM and CS1 (NOT) of ICS2 and 3 are connected to IC12's Q line. When this lire is low RAM becomes selected and data is passed to, or stored from the data bus according to the state of the R/W (read/write) line and selected address on lines A0 - A7. Il - I4 and output lines Ol - O4 are linked The input lines together on to the data bus and direction of data flow is controlled by the microprocessor timing logic via the MWR (NOT) line.

The CS2 line of RAM's IC3 and IC4 is a second chip select line which must be maintained at a 'l' level while the system is running. This line is used to ensure that RAM does not receive any incorrect data when the system is powered up or shut down. This is further covered under Section 2.2.2.4.4.2 as are the functions of D_1 , D_2 , D_{12} and the separate power supply to RAM via VDD RAM.

The microprocessor timing is set by a crystal (XL) with appropriate loading Cl and C2 and bias resistor Rl, as defined by the manufacturer. Design frequency is 2MHZ and was chosen based on the needs of the system. The operate frequency is limited by the working voltage and temperature range. The working voltage was chosen as 5V to suit the needs of the ROM. The design frequency gives adequate margin when the system operates at 85°C that allows sufficient time to execute all required system functions and allows memory components to run well inside their timing restraints. In addition, the relatively low operate frequency holds microprocessor power consumption to a low level.

Data bus lines D0 to D7 are connected to ground via pull down resistors R2 to R9 such that on power up and power down, data lines return to known states. This helps ensure that incorrect data is not passed to RAM, which would corrupt data held for GSE read out.

Resistor R10 and R11 act as pull up resistors for the two flag lines EF1 (NOT) and EF2 (NOT).

The microprocessor WAIT line is connected to VDD via the motherboard also CK IN and CK OUT are connected together via the motherboard, and all these connections are designed to facilitate board testing.

All other remaining microprocessor inputs and outputs, namely DMA IN (NOT), INT(NOT), SCO, SCl, EP1 (NOT) to EF4 (NOT), TPA, TPB, NO, N1, N2, CLR (NOT) and Q lines act as control or timing outputs or inputs as described in subsequent sections.

Capacitors C3 to C7 are filter capacitors placed strategically around the pcb to reduce effects of supply borne transients or induced pickup.

2.2.2.3 Logic Card

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(Circuit diagram reference 43761-142 CD (Master) - Reference 2-9 or 43761-148 CD (Slave) - Reference 2-10

The logic card can be sectioned into several areas having well defined functions to perform. They are power up, reset circuitry, input and output control, interrupt timing, head drive timing and control input data buffering and output data buffering.

2.2.2.3.1. Power up, Reset Circuit

To ensure correct system operation when power is first applied the circuit must be in a known state. Essentially all important microprocessor regis. s must be reset to zero, output ports must be cleared such that transient conditions do not appear at the CWU and some system flip flop registers must be set to a known state.

R1 and C1 form a time delay function and act in conjunction with R2, R3 and two buffer sections of IC2. When power is first applied, C1 is discharged. Via the pot chain divider of R2 and R3 the buffer input (pin 5 of IC20) is held at OV resulting in the clear line, CLR (NOT), output at pin 2 of IC20 being held

low. Note that since the resistor R3 of the pot divider chain is connected to the CLR (NOT) line, the pot divider is initially zero volt referenced.

The general requirement of the system is that the CLR (NOT) line should be held low for a short period of time to ensure correct reset of the above mentioned functions. As Rl causes Cl to charge up, the threshold of buffer input pin 5 is reached such that its output now changes to a 'l' state (5V level). The clear line follows this transition which is speeded up by the fact that the divider chain R2 and R3 is now 5V line referred effecting a schmitt trigger action. The transition effects the removal of the clear state from all attached circuits.

Buffer input pin 7 of IC20 is also connected to the clear line such that via its output, pin 6 and diode Dl, output port IC12 is initially cleared. The action of CS2 input on the output port IC12 is discussed in section 2.2.2.4.

2.2.2.3.2. Data bus Lines

Data bus lines connected to the microprocessor (external to the pcb) are connected to output port IC12, input ports IC14, IC15 and IC17 and to outputs of IC6 and IC10.

2.2.2.3.3. Data bus Control

Data being input to, or output from the microprocessor via the data bus lines is controlled by decode chip ICl3 which itself is controlled by timing and output signals generated by the microprocessor. Lines NO, Nl and N2 are input lines to the decoder chip which contain encoded data as to the required port (input or output) to or from which data is to be passed. ICl3 decodes the N lines and, its outputs are connected to chip enable lines of various input and output ports or act as clock lines. CKA and CKB inputs of ICl3 are connected to TPA and TPB outputs of the microprocessor controlling the duration that ICl3 outputs remain active.

2.2.2.3.4. Interrupt Timing

The system requires for correct operation an interrupt signal which occurs once every 832us. This signal is sent to the microprocessor's INT (NOT) (interrupt) input causing an interrupt software program to be executed.

To generate the timing signal the microprocessor's own timing pulse, TPB, is used. This pulse occurs every 4us with a crystal frequency of 2MHZ.

The circuit involved is IC1 and IC2.

The timing pulse TPB is connected to the clock input of ICl (pin l). With the EN line connected to VDD the counter chip causes TBP pulse to be divided by 16 at its output (pin 6). Thus, at this point a square wave of 64us period is observed. This waveform is applied to the enable (EN) input of the second counter stage of ICl. With the clock input (CK) connected to VSS the chip acts to increment the counter on the negative transition of the incoming signal.

The following operation is then discussed in conjunction with Figure 2-7.

Q3 output of IC1, by the divider action of IC1 is caused to change state on negative transitions of the previous binary divide stage, resulting in the pulse train shown. When Q4 output is low the positive transition of Q3 has no effect on the output Q (pin 1) of IC2, since at the transition the data input to IC2 at pin 5 (Q4 of IC1) is zero. When Q4 output is high, the positive transition of Q3 will cause a change of state at IC2 pin 1 to a '1'. The data input at pin 9 of IC2 is now at '1' level, consequently, at the next positive transition of this D type flip flop's clock input a '1' will be transferred to its Q output (pin 13.) As can be seen from the timing diagram, this occurs 32us later.

Pin 13 of IC2 acts as a reset input to the second stage of the divider chain of IC1, and one D type section of IC2. Because the D input at pin 9 of IC2 is now returned to 'O' by this reset action, then on the next positive transition of Q4 (pin 6) of IC1, the reset pulse is removed.

This cycle is repeated as shown by the timing diagram such that the Q output (pin 1) of IC2 is low for 800 us and high for 32us. Q (pin 2) of IC2 is the compliment of this and consequently applies a negative going edge to the INT (NOT) input of the microprocessor once every 832us. As can be seen this interrupt pulse is self resetting after being sustained for 32us. The timing of the microprocessor hardware and software is such that this interrupt pulse is always recognized before it has time to return to the standby state.

At power up the output states of ICS 1 and 2 are random which can cause an initial incorrect timing of the interrupt pulse. However, since the software program does not enable interrupt pulses to be recognized for some milliseconds after power up, the required synchronization has time to occur.

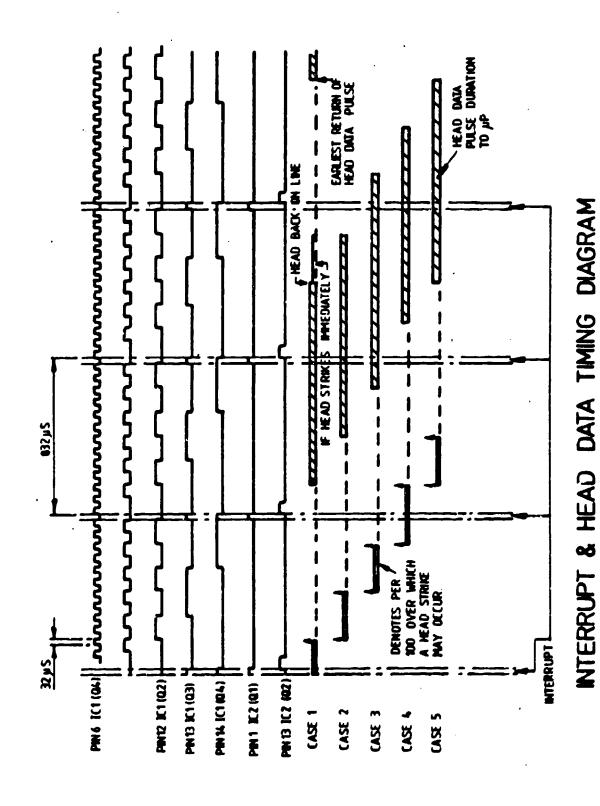


FIGURE 2-7

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2.2.2.3.5. Head Drive Control Circuit

The eight head drive circuits described under Section 2.2.2.3.1. each require individual control such that at the occurence of a strike, the head is starved of voltage for a 2ms period. ICS 3 - 10 and ICS 18 and 19 are responsible for head drive control and buffering on to the data bus for access by the microprocessor.

Circuit description considers one control section associated with head 1.Active components are R5, R32, ICl8 nand gate (with output pin 3), R43, IC3 NOR set/reset flip flop (with Q output pin 2), IC4 binary counter and IC6 transmission gate output pin 1 of which is connected to the data bus line D0.

Under standby conditions the set/reset flip flop has its Q output (pin 2 IC3) at a 'l' state since the last input would have been a set input.

Consequently, the reset input of the binary counter would be disabled and the clock pulse input at pin 1 (derived from the timing block) would have no effect. The output (pin 3) of the and gate is dependant on the input at pin 1. This, the time share signal is high ('1') for 167mS and low ('0') for 167mS repetitively. Therefore, R32 acting as the base current drive to TR7 of the head drive circuit controls whether the head is on line or off line.

When head 1 strikes, a pulse is developed across R5 due to the differentiating action of the combination of C9 (on the head drive card) and R5. This pulse acts as a reset pulse to the set/reset flip flop, causing its Q output to change to a 'O' state. At this time the time share input to the und gate (pin 1) is high (which it had to be to allow a strike to occur initially). The resulting 'O' state now existing on pin 2 of the nand gate causes its output to go to a '1' state, the result of which is that the striking head is starved of voltage.

The duration that the head is starved of voltage is a function of the operation of the binary counter IC4. The counter is clocked by pin 12 (Q2) of IC1, a pulse which occurs once every 256ms as shown on the timing diagram Figure 2.7.

Again, with reference to the timing diagram, when a strike has occurred the reset input R (pin 7, IC4) is released allowing the CK input to cause the counter to count.

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When eight CK pulses (low to high transitions) have elapsed Q4 output of the binary divider goes high. Since this output is connected as the set input of the set/reset flip flop the effect is to cause the binary divider to be reset and to restore the head back to an on line status. Since one clock pulse is normally 256us, then it follows that the head has been off line for 2048us or just over 2ms.

The timing diagram shows that this software is subject to some variation due to the uncertainty of when the head will strike with respect to the fixed timing intervals of the clocking pulse.

The timing diagram shows the 5 cases which can occur indicating the range of strike time between clock pulse events, the result of which is that head 'off time' can vary between 1.92mS and 2.24mS.

The Q3 output of the binary counter is used to act as an indication to the microprocesor that a head has fired. This Q3 output is fed to a transmission gate which controls Q3 access to the data bus, the control line of which is conected to output 7 (07) of ICl3. Head status is available to the microprocessor by executing a command on INPUT PORT 7.

To ensure correct interpretation of the incoming data, the timing of the circuit and manipulation of the data is critical.

Again, with reference to the timing diagram it can be seen that the Q3 output (which indicates a head strike to the data bus) can occur in such a way as to either be true at one or two successive interrupts. The interrupt marker causes the interrupt program to input the head status data to the microprocessor, thus it could be that the system interprets one strike as two events if the event happens to "straddle" two interrupt markers.

As shown by case 1, when the head returns to an on line status Q3 output cannot return to a state showing a second strike event until just before the fifth interrupt event. For this case and all other cases it is proven that two separate head strikes on one head cannot be observed by two consecutive interrupt markers. As a result the software program is written so as to disregard as false, a second pulse if two consecutive strikes occur.

2.2.2.3.6. DMA and Control Data Parameters

Direct Memory Access (DMA) is utilized in the design to pass relevant data from one processor to the other. This data includes a byte of information containing parity bits and various status bits, to be discussed under the heading, Software. In addition each processor transmits to the second processor a byte containing the status of each head such that the receiver can make appropriate logic decisions.

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DMA transfer is used such that the important task of observing fire conditions (termed the "gathering phase") is not interrupted. DMA causes the transfer of the above data directly to the receiving processors memory and is virtually unseen by the normal interrupt program. To guarantee that the data is received correctly the hardware associated with the DMA function is duplicated in such a way that if one of the receivers is faulty it can be identified.

The circuitry associated with the DMA activity is essentially ICl5, 16, 17, 22 and 23 and associated components.

The transfer of data is effected by the sending microprocessor, the result of which is that the required level to be transmitted appears at the receiving logic card via the DMA DATA IN line (pin 53 on the edge connector). A clock pulse is required to initiate the receiving processors DMA mechanism. The clock pulse is generated by the sending processor and appears at pin 17 of the receiver logic card designated DMA DATA CK IN.

The DMA DATA IN logic level is buffered and separated by two buffers of IC21. The outputs of both buffers are connected, one to each of the two input ports IC15 and IC17 associated with DMA transfer both being connected to the 0 input.

The remaining inputs to the two DMA input ports are:

bit 1 (I1) = master/slave initialization bit.

bit 2 (I2) = port identity bit.

bit 3 (I3) = third level adjacency bit.

bit 4,5,6, (I4,I5,I6) = second level adjacency bit.

bit 7 (17) = first level adjacency bit.

Master slave initialization bit is required to ensure that at switch on the software takes a path such that the time share for side 1 and side 2 of the system functions in antiphase to each other. The only difference between logic cards 43761-142 (Master) and 43761-148 (Slave) is in the setting of the master/slave bit, master is recognized as being connected to a '1' level and slave as being connected to a '0' level.

The port identity bit I2 is connected to VDD on ICl5 input and to VSS on ICl7 input. This is to enable the processor to recognize that it is correctly receiving data from both input ports.

The function of bits I3, to I7 are considered in detail in Appendix λ -1.

Each bit of transmitted data is transmitted twice and the receiving input ports are arranged by hardware means such that the data is passed alternately via IC15 and IC17.

Since two bytes of information are to be transferred twice, it follows that 32 separate DMA transfers occur requiring 32 memory locations in the receiver memory map.

When a DMA data transfer is intiated by the sending processor the required logic level is placed on the DMA DATA IN line. When it subsequently initiates a clock pulse at the DMA DATA CK IN the following events occur.

R40 connected to the DMA DATA CK IN line acts as a load resistor to the transmitting circuit which in the non sending mode is in a tri-state high impedance mode. The incoming high level pulse is differentiated by C2 and R29 and then, via isolating diode D5 and associated bias resistor R31, is connected to the C (clock) input of IC16.

The used half of ICl6, a D type flip flop, functions with its D input connected to its Q output, i.e. such that it operates in a divide by two mode.

Assuming that Q of ICl6 is initially '1', then at the event of a positive transition on its C input, the Q output changes to a '1' state, thus ICl5's CS2 input (chip select) becomes enabled. At the same time ICl5's CK input has changed from a '1' to a '0' level. The transition causes the data on lines IO to I7 to be latched into the port and a low level on the service request output SR(NOT) to occur.

SCO and SCl are outputs from the processor which indicate whether the processor is performing a fetch, execute, interrupt or DMA activity, when carrying out a DMA activity . SCO = O and SCI = 1.

At the moment SR (NOT) goes low, the state of the system is not a DMA cycle, as a result the NOR gate connected to SCO and SCI (IC22 and IC23) cause a '1' state at pin 2 of IC23. Thus, the output (pin 3, IC23) of the NOR gate changes to a high level ('l'). A 'l' level now exists at pin J of IC23, and since the SR (NOT) of IC17 has not been set to '0' then pin 6 of IC23 is a '0'. As a result of the transition of SR (NOT) from a 'l' to a '0' level pin 4 of IC23 changes to a '0'. This signal is transferred to the microprocessor on its DMA IN (NOT) input which it recognizes as a request to DMA information into its memory. The internal logic of the microprocessor waits until the next system execute cycle has been completed and then suspends normal processor operation for one system cycle such that DMA may be executed. On doing so, the state code SCO = 0 and SCl = 1 is applied to the NOR logic gates of IC22 and IC23 resulting in pin 11 of IC23 changing from a '0' state to a '1' state. With the condition CS1 and CS2 at '1' status the input data is enabled onto the data bus and subsequently due to logic action within the processor is stored at a defined memory location.

At the completion of the cycle the SCO and SCI state revert to the code defining the next 'fetch' phase of operation, resulting in IC23 pin 11 output changing to a '0' state. The internal logic of the input port uses this transition to reset the SR (NOT) output to a '1' standby state, However, due to the finite delay between CS1 going negative and the reset of the SR output a condition exists at inputs 1 and 2 of IC23 whereby a second transient '1' pulse can occur. This race condition would activate incorrectly another DMA request at the microprocessor. To eliminate this timing problem, small capacitors are connected between IC23 pin 3 and ground and similarly between IC23 pin 3 and ground, namely ClO and C11. This short time delay effected by the gate output impedence in conjunction with the capacitor is sufficiently long to eliminate the effects of the reset delay propagation time of the input ports service request flip flop.

A second DMA DATA CK IN pulse would then have the effect of causing data to be input via IC17 due to the toggling action of IC16.

Because the program software needs to know the status of the master/slave bit of the input data before a DMA activity takes place, the hardware is arranged such that this data may be input by alternative means.

A second path to initiate the DMA process is included using an initializing clocking pulse derived from pin 6 of decoder chip ICl3. This output is differentiated by C3 and R30, then via isolating diode D4 is applied to the C input of ICl6 in similar manner to the DMA DATA CK IN input. By executing an output instruction to port 1 (which does not physically exist) a 2.75us active clock pulse is produced initiating DMA activity.

2.2.2.3.7. Input Data Buffer

Input data is received by the data bus from three sources:

- Via IC6 and 7 which is head status data, as previously described.
- 2) By ports IC15 and IC16 acting in DMA mode, as previously described.
- 3) By IC14.

ICl4 is a hex inverter/buffer with tri state output and is used to pass six control signals to the microprocessor. When its OD input is high ('l') its outputs are in high impedance mode, when the OD output is low input data is inverted and accesses the data bus. When an input instruction on input port 3 is executed by the microprocessor program, pin 7 of ICl3 goes high for 2.75us and via the inverting buffer of IC22 enables the data output onto the data bus.

The six input control signals are as follows:

- a) D5 input gives the microprocessor the status of the fire test switch. D5 receives this signal via the circuit involving R28, R25 and D2. When the fire test button is in a standby state a OV level exists at the fire test input to the logic card (edge connector pin 1). D2 is then forward biased taking current through R25 and off card resulting in D5 input to ICl4 being at approximately 0.6 volts. When a fire test is requested the FIRE TEST input to the card will be at 7 volts. D2 now acts to block the 7V signal and the pull up resistor R25 serves to pull the D5 input to a '1' level.
- b) D2 input gives the microprocessor access to the status of the fault test switch. The fault rest input at pin 2 of the logic card edge connector is 0v in standby mode and at 7v when the fault test button is depressed. Associated components R27, D3 and R22 act in similar manner to that described for fire test input.
- c) Inputs D1, D3, D4, and D6 of ICl4 are associated with GSE (ground support equipment) operation. All four inputs are tied by pull up resistors to the system VDD rail by R21, R33, R24 and R26 respectively. In normal operating conditions, i.e. when GSE is not connected, the four GSE inputs to the logic card are open circuit, therefore, D1, D3, D4 and D6 present logic level '1's to the ICl4.

The four GSE inputs allow the CCU operation to be controlled by the ground support equipment. Combinations of logic levels applied to these inputs select different programs for running. These programs are initialized by resetting the system causing the software program to interrogate the four GSE inputs and subsequently to run the required program.

System reset is effected by discharging Cl through D6 from the GSE RESET input at pin 41 of the logic card edge connector.

The above inputs are connected to the data bus via IC14 Q outputs as follows:

Input	Connected to	Data Bus
GSE 1		bit 0
FAULT SWITCH		bit 1
GSE 3		bit 2
GSE 2		bit 3
FIRE SWITCH		bit 4
GSE 4		bit 5

2.2.2.3.8. Output Data Buffer

Output data buffering (and latching) is effected by ICll, 12, 20 and 21. ICl2's inputs are connected to the data bus. Data being latched into the port is controlled by CSl, CS2 and CK inputs. The mode input of ICl2 is connected to VDD to characterize the device as an output port. With CSl permanently connected to VSS the chip select has only to be satisfied by CS2 = 1 for data bus information to be latched into the ports outputs at the next occurence of a CK pulse. The microprocessor selects this output by an output instruction to port 4 which causes decoder chip ICl3 to issue a 2.75us pulse at pin 12. This output is connected to ICl2's CS2 input. The microprocessor then issues the required data to the data bus and timing pulse TPB which is connected as the CK input to ICl2, effects the data latch.

The eight outputs from output port 4 (ICl2) all have pull up load resistors connected (R13 to R20). Port bit operation is as follows:

O7 output (pin 12). This output is the time share output, a square wave pulse train generated by the system program. The time share waveform has a period of 334mS, 167mS high and 167mS low.

The time share waveform is fed via a buffer stage of IC21 and R4 to the head drive card which is then utilized to control high

voltage at the heads. The time share output is also fed via ICll's 'D' input and H output, this chip acts as a buffer to its input signals. With END input tied permanently to VDD input data is buffered directly to its output at H. This line is connected to a flag input on the opposite side microprocessor card (EF2) (NOT) and is used for monitoring.

O6 output (pin 19) and O4 (pin 15). These outputs, GSE2 and GSE 1, are each buffered by a buffer of IC21 and are connected to the CCU GSE plug. Both outputs transmit signals to the ground support equipment as confirmation of execution or at completion of execution of required program as dictated by the GSE I/P control lines.

When the system runs a fire detection program, software caused the GSE 1 line to follow the time share signal and the GSE 2 line to be at a '1' state only during when a head test is being performed. This operation is further described under the heading "Software".

05 output (pin 7). This output is buffered by a buffer of IC21 the output of which controls power to the emitter via the head drive card as described in Section 2.2.2.1.

O3 output (pin 15) is an output called INHIBIT OUT. This signal is used as an inhibit signal on the common logic card; under standby conditions this output is at Ov. O3 is connected to the ENC input of IC11 which with a Ov on its input causes output 6 to be high impedance. When O3 changes to a '1' output, data at IC11's C input is transferred to the G output. Because C is connected to VSS, a change at G from high impedance to a '0' state will occur. This output is also crees connected to the second microprocessor via the processor cards EF1 (NOT) input and is used by the software program. Further operation of the inhibit function is described in Section 2.2.2.4. and in the section headed "Software".

O2 output (pin 7). This output is the FIRE output which in standby conditions is at Ov, and at Pire conditions changes to a '1' state. The output is fed to the common logic card described in Section 2.2.2.4.

Ol output (pin (). This output is the FAULT output which in standby conditions is at Ov. When a fault is issued the output changes to a 'l' state. This output is fed to the common logic card as described in Section 2.2.2.4.

Of output (pin A). This output is termed DMA DATA OUT. Onto this output is loaded data to be transferred to the second microprocessor. ICll acts as a buffer. With ENB connected to VDD, data at F follows data at B. The DMA DATA OUT line is then connected to DMA DATA CLOCK IN on the second microprocessor.

DMA DATA CK OUT at pin 19 of the logic card edge connector is derived via a buffering section of IC11 from a decoded output of IC13, which acts as the clock output for DMA data. DMA DATA CK OUT is connected to the second microprocessor as DMA DATA CK IN (see CCU circuit diagram 53813-203CD). (Reference 2-5.)

ICll buffering also acts as a device to eliminate effects of differences in supply voltage of each microprocessor. ICll allows level shifting to occur by connecting its VDD terminal to the positive supply of the processor recieving data and the VCC terminal to the positive supply of the processor sending data. Note all four outputs of ICll are cross connected to the second microprocessor circuit.

The Q line output from the microprocessor is connected to a buffer on the logic card, this path is via edge connector pin 32 and buffer input pin 9 of IC20. The buffered output is connected to edge connector pin 33 and is termed GSE DATA. This line is connected to the GSE plug on the CCU and is used to transfer serial data from the processor memory to the ground support equipment.

2.2.2.3.9. Filtering

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Capacitors C4 to C9 are connected in strategic positions across the power supply lines to filter out unwanted spurious supply borne signals and noise elements.

2.2.2.4. Common Logic Card (System A)

(Circuit diagram reference 43761-144CD) - Trence 2-11

The common logic card for a system A (dual microprocessor system) consists of three independent circuits.

- a) Logic associated with fire and fault indication.
- Driver circuits to energize output relays.
- c) Circuitry which performs buffering and level shifting as inputs from the CWU.
- d) Circuitry which detects impending switch off of power to the system.
- e) Filtering circuitry.

2.2.2.4.1. Fire and Fault 10

re and fault logic is we ermined by ICl, 2 and 4 and associated appoints.

Power for ICl, 2 and 4 is obtained by "ORING" both microprocessors 2. Lupply rails. Note that the circuit diagram refers to 'A' 5.6v and B' 5.6v refering to Side A and Side B of an 'A' type system.

D1 and D2 perform the power supply "ORING" function which is necessary such that if one procesor side power supply fails for any reason, the common logic card will still be capable of logic decisions based on the remaining good 5.6v rail.

As described in section 2.2.2.3.8, fire and fault inputs (for both sides A and B) are in the 'O' state in standby conditions. The inhibit inputs for both sides are in a high impedance mode.

Consider the inputs to ICl, with (A) FIRE OUT at 'O' pin 8 of ICl via the inverter will be at 'l'. The second input to this NAND gate at pin 9 will be 'l' because (A) INHIBIT IN is high impedance and Rll acts as a pull up resistor. Consequently, NAND output pin 10 will normally be at 'O'.

Similarly, considering (B) FIRE OUT and (B) INHIBIT IN input to IC2, pin 10 of IC2 will normally be in the 'O' state.

NAND gate output, pin 4 of IC4 will therefore normally be at a '1'. This NAND gate of IC4 acts to effectively AND together fire conditions from both sides of the system.

When a fire is indicated by A FIRE OUT and B FIRE OUT both input pins 5 and 6 of IC4 will change to a 'l' state causing the ouput pin 4 to change to a 'O' state. If, however, only one FIRE OUT changes to a 'l' state the AND logic is not satisfied and pin 4 of IC4 stays at a standby 'l' state.

Fault logic is similar to that of FIRE logic, (A) FAULT OUT and (B) FAULT OUT under standby conditions cause 'O' level inputs at pins 1 and 2 of IC4, therefore with no fault condition present, pin 3 of IC4 is at a '1' level. For a 'O' output on pin 2 of IC4 both microprocessor FAULT OUT lines must signal a '1' (fault) level.

If one side of the system is shut off by the second side the AND fire and fault logic must effectivley change to OR. In the event of a side shut down by the second side, that second side will issue a 'l' level at the inhibit output of port 4 on the logic card, which causes a change from high impedance to a 'O' state on (A) or (B) INHIBIT IN line of the common logic card.

Take the example where side A processor has caused side B to shut down and caused (B) INHIBIT IN to change to a 'O' state (Note that (B) INHIBIT IN is an input from side A logic card port 4 as can be seen from CCU circuit diagram). With (B) INHIBIT IN now changed to a 'O' state pin 10 and pin 11 of IC2 will be to a 'l' state.

The occurence of a FIRE condition ('1') at (A) FIRE OUT now causes pin 4 of IC4 to change to a '0' state. Similarly, the occurence of a FAULT condition (1) at (A) FAULT OUT now causes pin 3 of IC4 to change to a '0' state, effectively changing the gates function from AND to OR.

An identical logical operation is performed if side B causes side A to shut down, in that only B FIRE or FAULT lines need to change state to effect a transition at the output NAND gates of IC4.

2.2.2.4.2. Logic Drive and Output Circuit

Prom section 2.2.2.4.1., in the event of a fire condition IC4 pin 4 changes from a '1' state to a '0' state, and in the event of a fault IC4 pin 3 changes from a '1' to a '0' state.

2.2.2.4.2.1. Fault Condition

With no fault condition TR2 receives base current drive through R19 which in turn enables base current drive through TR3 via R27 and the conducting TR2. TR4 will also be switched on since its base current will flow through R29 and the conducting TR3. With TR4 switched on RLA will be energized via the 28v supply rail which feeds the logic driver stage.

With relay RLA normally energized at standby relay contacts RLA 1 and RLA 2 are open. Isolating diodes D14 and D15 are commoned together by their cathodes to comprise the fault drive output to the CWU. The isolating diodes are included such that relay contacts may be checked individually by GSE via the check points lines at edge connector pins 36 and 34.

When a fault condition occurs TR2 will turn off, TR3 turn on and TR4 turn off causing RLA to de-energize issuing a fault condition to the CWU.

2.2.2.4.2.2. Fire Condition

With no fire condition, TRl receives base drive via R20 turning TRl on. With TRl collector developing only its saturation voltage base current supplied by R25 to TR5 is diverted through TRl thus TR5 is switched off. Under standby conditions, i.e. with the fault state at standby TR6 wll be switched on as TR3 is normally on.

When a fire input occurs TR1 will switch off causing R25 to feed base current to TR5. With TR5 and TR6 on RLB will energize via TR7 emitter base junction causing TR7 to switch on passing its collector load current through R34 to ground.

TR7 acts as a sensing circuit used to pass a confirmation signal back to the microprocessor indicating that the fire condition has successfully been initiated. With TR7 off, i.e. no fire condition, current flows from the A side VDD rail via R7, D3 and R34 and from the B side VDD rail via R8,D4 and R34 to ground. With R7 and R8 each 100k and R34 at 2.7K the anodes of D3 and D4 will be approximately one diode drop above the 0v rail. This FIRE TEST VERIFY and is connected to EF4 (NOT) input on the microprocessor card. For the second side the signal at D4 anode is taken via R2 to its EF4 (NOT) input on the microprocessor card.

When a fire signal is issued by the system TR7 turns on, connecting TR7 collector to the 28v rail. This reverse biases D3 and D4 causing R7/R1 and R8/R2 combinations to act as a pull up resistor on the microprocessor flag inputs. Therefore, when a fire condition occurs microprocessor EF4 (NOT) inputs change from a 'O' to a 'l' state.

2.2.2.4.2.3. Fault Override

With the series connections of TR5 and TR6, if a fire condition is being indicated a subsequent fault condition causing TR6 to switch off will make the fire condition at the CWU clear and indicate a fault condition, i.e. a fault condition overrides a fire condition.

2.2.2.4.3. Inputs from CWU

The CWU (as described in section 2.3) effects closure of a switch to the 28v rail if the fire test button is depressed and closure of a second switch to the 28v rail if the fault test button is depressed.

The fire and fault test inputs are routed to the FIRE TEST I/P and FAULT TEST I/P on the common logic cards.

With neither test button depressed both transistors TR8 and TR9, are switched off and both the FAULT TEST and FIRE TEST lines fed to the logic board, are at Ov.

When the fire test button is depressed R39 passes current because pin 22 of the common logic card edge connector is conneced to 28v at the CWU. D16, a 7.5v zener diode clamps the voltage level at the base of TR9, which, with R37, acts as an emitter follower stage. The voltage at TR9 emitter is then approximately 7 volts. Similarly, when the fault test button is depressed, a change of voltage from 0v to about 7 volts occurs at TR8 emitter.

Components C12 and C13 in conjunction with R39, R41, D16 and D17 act to eliminate interference entering the circuit via the cable connectors from the CWU.

2.2.2.4.4. Low Supply Voltage Detection

2.2.2.4.4.1. The Need For Low Voltage Detection

Low voltage detection is required to ensure correct operation of the system in the event of short duration loss of power and to ensure that memory data is not corrupted as discussed in section 2.2.2.2.

2.2.2.4.4.2. Operation of Low Voltage Detection Circuit

The circuit consists essentially of the quad comparator IC3 and associated components. The battery card (described in section 2.2.2.6.) supplies, under full charge conditions, a 4 volt power source to pin 26 of the common logic card edge connector.

(A) VDD RAM is a 5v input supply from the head drive card, this supply is fed via D18 as the supply voltage to the comparator IC3. Similarly (B) VDD RAM is fed via D19 to the comparator supply input. Operation is then such that if A supply fails the comparator continues to function due to the sustained presence of B supply, and vice versa. The battery input is connected directly to the comparator VDD input but high current does not flow from the VDD RAM line (at 5V) to the battery (4V) because a blocking diode is included on the battery card output line (See section 2.2.2.6.).

D18 and D19 are included such that in the absence of the battery (in production, since the battery card feature in for flight trials purposes only) VDD of IC3 receives current from either A side or B side VDD RAM supplies.

D7 clamps the battery voltage to 7.5V in the event of an open circuit battery, protecting the comparator and components which it controls.

Detection occurs seperately for side A and side B of system A, operation of which is identical, the following describes the operation of Side A low voltage detection.

Resistor chain R5 and R6 acts as a potential divider reference voltage which is fed to the inverting input, pin 4, of the quad comparator, this voltage is 1.25 volts. The non inverting input pin 5 of IC3 is connected to the low voltage detection arm of the bridge on the head drive card. (See circuit diagram 43761-143 CD) Under normal conditions the voltage is greater than 1.25 volts.

The potential divider chain of D10,R2, R3,and R71 on the head drive card is set such that the voltage at the R2, R3 and R71 node is 1.25 volts when the unregulated supply voltage (at D10 anode) is 8.1 volts.

At this unregulated voltage the 5V regulator on the head drive card functions correctly, however to obtain a voltage of 8.1 volts implies that the 115V supply has fallen below 85 volts A.C., this in turn affects the high voltage to the heads, below this supply voltage heads may not fire correctly. The action of the low voltage detection circuit eliminates this unwanted condition.

At normal conditions with Pin 5 of IC3 greater than 1.25 volts the collector transistor output at pin 2 of IC3 will be off.

A second low voltage detection circuit is that formed by the potential divider of R23 and R24 which feeds comparator inputs, pins 9 and 11. The Inverting inputs of these two comparators are connected to the 1.25V reference point. This detection network acts to detect the presence of the 28V supply. When the 28V supply is present the voltage at R23/R24 node is greater than 3 volts. Under all normal fluctuations of the supply rail, therefore, the transistor outputs at pins 13 and 14 of IC3 will be switched off.

IC3 pin 4 output is connected to IC3 pin 2 output both having a common pull up resistor R13. With both output transistors switched off, R13 causes the CS2 line, connected to these outputs to be at VDD RAM voltage.

If the 115V A.C. supply drops below 85 volts the voltage at pin 5 of IC3 will drop below 1.25 volts causing the output state of the comparator to change, a 0V condition will now exist at the CS2 line.

Alternatively if the 28V supply falls below approximately 8 volts, pin 9 of IC3 will now be less than 1.25 volts causing the output state of the comparator, pin 14 to change, again an OV condition will result on the CS2 line.

Therefore, either a drop in AC line voltage or a loss of the 28v supply voltage causes the CS2 line to change from a 'l' state to a '0' state.

Capacitor C2 ensures that VDD RAM voltage stays high for sufficient time for the correct comparator operation i.e. so that the comparator reference voltage is held high for a short period after the VDD RAM regulator input has dropped such that correct regulator is not taking place.

Assuming that the system has just been switched off, CS2 will change from a 'l' state to a '0' state. As VDD RAM voltage collapses the VDD input to IC3 will be powered via the battery input. The VDD line now has battery voltage which is also fed to RAM memory on the microprocessor card, thus maintaining memory content. The change of state of CS2 to a '0' via Dl state disables the CS2 input of RAM memory on the microprocessor card, a change which must occur before the supply voltage drops out of range of that specified for correct operation of the microprocessor chip. For the system design the CS2 change of state to a '0' level occurs approximately 2mS before the 5v supply rail (VDD) begins to drop out of regulation.

The action of CS2 changing state also has effects on the logic card (see circuit diagram). The CS2 line via Dl of the logic card, causes the power-on reset capacitor to be discharged when CS2 changes to a '0' state, holding the CLR line at a reset state during the power-off period.

When power is restored to the system the following sequence of events occurs: VDD RAM line voltage will change from battery voltage to its normal running voltage level. At the same time, dependant on how quickly supply voltage on AC and DC supplies builds up, CS2 line will change to a 'l' state. This will cause Dl on the logic card to become reverse biased allowing the power-on reset circuit to function. Subsequent removal of the reset condition causes D2 on the microprocessor card to become reverse biased and R12 causes CS2 to be pulled to a 'l' level allowing RAM memory to become enabled.

This sequence of events ensures that all timing and initialization needs of the system are met.

2.2.2.4.5. Piltering Circuit

Diode D8 is an energy absorbing zener diode which clips incoming high voltage spikes. To keep power dissipation of D8 to safe limits yet allow all voltage requirements of the logic drive circuit to be met a fusible resistor of 15 ohm impedance is included in series with the 28v supply rail.

Diode D11 in series with the positive supply rail cuts off any effects of high negative voltage excursions on the 28v supply line.

Capacitors C3 to C11, C14 and C15 are active in reducing unwanted circuit interference.

2.2.2.5. Common Logic Card (System B)

(Circuit diagram reference 43761-146CD) - Reference 2-12

System B common logic card uses the same pcb as that for System A with minor amendments. The amendments are to make links at comparator IC3 such that the B side low voltage line detection circuitry is inactive, and to eliminate a NAND gate package (IC2 on System A common logic card) and associated resistors.

With the of IC2, operation of the fire and fault logic is as if A side has effected an inhibit on B side logic gating.

Afl other functions are as per System A common logic card description.

2.2.2.6. Battery Card

(Circuit component reference 43761-140CD) - Reference 2-13

The battery card is resident in System B only. It consists of two independant battery circuits suppling, in the case of Battery A output, power to System A common logic card battery input. This is performed by a connecting wire in the system harness on the aircraft installation.

Battery B supplies power to System B common logic card Battery input via the CCU mother board.

The battery cells B1 to B6 are sealed nickel cadmium cells with a 240mAH rating. A trickle charge current is fed to the cells via either D1 and R1 for cells B1 - B3 or D2 and R2 for cells B1 - B6. Isolating diodes D3 and D4 then pass battery current to the common logic card and RAM on the microprocesor card.

Design of the battery card was based on an average flight envelope of one and a half hours. Thus, to ensure that sufficient charge is stored during this period a relatively high trickle current is necessary. To attain this, a 240maH rating battery had to be used to ensure that over the operating temperature range the maximum allowable trickle current was not exceeded. The design ensures that a battery will supply the comparator on the common logic card and the RAM on the microprocessor card for 8 hours after a normal flight envelope.

It should be noted that the battery card is included only for flight trails and has an operating temperature range limited to -30° to $+45^{\circ}$.

2.2.2.7. Filter Board

(Circuit diagram Ref: System A 43765-028, System B 43765-029) - References 2-14 and 2-15.

It is necessary for the control unit to meet the conducted emission, susceptability and transient requirements of MIL-STD-461A and MIL-STD-704A. This is acheived by three filter networks on the filter board for System A and two filter networks on the filter board for System B. To minimize the radiated emission effect of the incoming supply leads, the filter boards are mounted as close to the plug as possible.

There are two 115v filters on System A, and one 28v DC filter. The 115v filters are designated 115vA and 115vB. The components that make up 115vA are R1, D1, D2, D3 and D4 (transient voltage suppressors) R1,R3 and C2. D1 and D2 clip the incoming transient voltage on one half cycle to approximately 350v peak and D3 and D4 clip the voltage on the following half cycle. R1 provides some source impedance for the transient voltage suppressors to limit the current flowing during the transients. R1 is a fusible resistor which will blow if the circuit exceeds a constant

current of approximately 0.65A. R3 and C2 act as a radio frequency suppressor. Similarly, components D5, D6, D7, D8, R2, R4 and C3 make up the 115vB filter. The 28v filter is made up of three components on the filter board. L1 and L2 slow up incoming and outgoing current transients, and C1 suppresses incoming voltage spikes. Further filtering of the 20v DC supply is carried out on the common logic card as discussed in Section 2.2.2.4. Similarly, System B has the same filter with the exception of 115vB which is not required.

2.3. Crew Warning Unit (CWU)

(Circuit diagrams ref. 53813-202-CD) - Reference 2-16

The Crew Warning Unit gives visual indication if either a fire or a fault is detected on either of the aircrafts engine fire detection systems.

2.3.1. Construction

General assembly drawing 53813-202A shows the units construction which is contained in a rectangular box made from stainless steel. The front panel is (2") high x (6") wide, and is retained to the box by means of two screws. On the front panel are six switch/indicator assemblies mounted in three groups of two. The outer two groups are indicators and the inner groups are switches. There are also four pillars mounted on this panel which support a circuit board and the remaining components. The switch indicator assemblies are connected to the circuit board and to a square flange bayonet recepticle by means of P.T.F.E. wire. This recepticle is bolted to the inside of the bottom of the box by means of four screws. The cable harness is of sufficient length to allow the four panel assemblies to be removed from the box to enable any necessary repairs.

The indications are of the sunlight readable type to MIL-S-22885/90 and the legends "FIRE" and "FIRE DET-FAIL" are only visible when illuminated. As these indication/switches are not of the waterproof type it is necessary to have drainage holes on each corner of the bottom of the box.

The unit is mounted in the aircraft by means of four D2US fasteners, two on each side of the front panel.

The unit has a natural polished finish apart from the front panel which is painted matt black, and has an overall size of 6" wide x 1.75" high x 5" deep. The approximate weight of the unit is 600g.

2.3.2. Circuit Description

The crew warning unit performs three functions:

- i) Fire and fault indication.
- ii) Fire and fault test.
- iii) CCU reset.

2.3.2.1. Fire and Fault Indication

For increased reliability, LP1 - LP4 are wires in parallel and provide the left engine "PIRE" indication when supplied by a 24 volt signal from the common logic card in the left engines control unit. Similarly, LP5 - LP8 provide the left engine "FIRE DET FAIL" indication.

LP9 - LP12 provide the right engine "FIRE DET FAIL" indication when supplied by 24 volt signals from the common logic card in the right engines control unit. Similarly, LP13 - 16 provide the right engine "FIRE DET FAIL" indication.

2.3.2.2. Pire and Fault Test

There are two test button facilities "FIRE DET TEST" and "FAIL IND TEST". The first test button "FIRE DET TEST" is a two pole normally open momentary action switch Sl. When the switch is depressed, Sla contacts close and supply 24volts to the fire test input on both common logic cards via Dl and D2 isolation diodes. This action energizes the test emitters as detailed in Section 3.4.3.2., and both FIRE indicators light.

The second test button "FAIL IND TEST", is also a two pole normally open momentary action switch, S2. When the switch is depressed, S2a contacts close and supply 24v to the fault test input on both common logic cards via D3 and D4 isolation diodes. This action generates a fault as described in Section 3.4.3.2., and both "FAIL IND TEST" indicators light.

The 24v that supplies these switches is filtered to minimize radio frequency pick-up. D5 is a reverse voltage protection diode. L1 suppresses the radio frequency currents and C1 decouples the radio frequency voltages.

2.3.2.3. Control Unit Reset

The "FIRE DET TEST" and "FAIL IND TEST" to switch provides a second function. When the control units \(\) is a fault mode it is necessary to reset them. This can be achieved by depressing these switches in a particular sequence as described in Volume I. S2b connects control line 2 to 0v and S1b connects control line 2 to control line 1. Control lines 1 and 2 feed to both control units as shown in installation drawing 222004. (Reference 2-17)

3.0 SOFTWARE DESIGN

An overview of the software system is given in para. 3.1 followed by more detailed discussion of the software segments.

3.1. Overview of Software

The system software resident in 3K bytes of ROM memory serves to control timing functions of the system, to process and act on fire data and to effect many system tests designed to prove the integrity of the system.

The assembled program listings are contained in Appendix A-2, all software description refers to the relevant program and should be read in conjunction with the system flow diagram 53813-203 and 204 FD. (Reference 3-1)

Program structure is such that the majority of functions occur under interrupt control due to the time dependant nature of the system requirements.

3.1.1 Software Component Programs

A cyclic operation occurs after the INITIALIZATION program has been completed, in which the two sides of the system (if System A) are synchronized and all required registers and memory locations are set to initial values.

After initialization the BACKGROUND program is entered, the primary function of which is to carry out tests to prove that ROM memory is not corrupt. This program is interrupted at intervals of 832 us to carry out the INTERRUPT program.

The interrupt program has two phases, GATHER and PROCESS, both are responsible for system timing. During the gather phase the sides time share is high and at each interrupt event the main function is to obtain head data. This phase lasts for 167ms.

On completion of the gather phase the time share changes to a low level and the PROCESS phase commences, this also lasts for 167ms.

At each interupt event during the process phase, system timing and system interrupts are monitored.

The PIRE program is responsible for processing the head data and computing if a fire or fault condition is to be set or reset. The fire program is executed after the gather phase of the interrupt program and is entered from the background program. Consequently the fire program is interrupted every 832 us meanwhile background operation is suspended. Upon fire program completion background operation resumes.

The final major element of the software is the GSE program which is executed upon command of the remote test equipment.

3.1.2 Program Development

All programs were edited and assembled using an RCA development system apart from the fire program and parts of the GSE program which were compiled using a tie to a main frame computer.

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Main frame written program was debugged in the same medium and then combined with the remaining program which was then debugged using the RCA development system and associated emulator.

3.1.3 Program Instructions and Language

Appendix A-3 contains a summary of the instruction set and their function of the 1802 microprocessor.

Appendix A-4 summarizes the level 2 assembly language used in the listing of the fire and part of GSE program.

3.1.4 RAM Memory Allocation

Fig. 3-1 maps the useage of memory locations in the RAM area between locations OCOO and OCFF.

3.1.5 Register Allocation

Fig.3-2 shows the major useage of microprocessor registers.

3.1.6 Plags and Interrupt Data

The major memory locations utilized for flags and input data is shown in Table 3-1 where individual bit useage is identified.

3.2. Initialization Program

The function of the initialization program is to set registers and memory locations such that upon entry to background, interrupt and fire programs, correct program operation occurs.

The second main function of the initialization program is to cause correct start up and phasing of the two processor sides if the system is A type.

3.2.1. Memory Locations and Register Initialization

At start up interrupts are disabled (line 4) and program control is moved to register P7 (line 10) Power-on reset causes program counter R0 to be reset to H'0000' and program runs from this program step under control of R0. Operation must be moved away from R0 control because the DMA capability utilized by the hardware required R0 to act as a memory pointer to which data is being passed.

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REGISTER	USEAGE
RO	DHA Memory Pointer
R1	Interrupt Program
R2	Stack Pointer
R3	Background Program
R4	Used By Interrupt Program
R5	Lower Half Used As Interrupt Timer Upper Half Used As Temporary Store In Interrupt Program
R6	Used By DMA Program
R7	Initialization & GSE Program
R8	Used As Subroutine Pointer
R9	Used As Subroutine Pointer
RA	Used By Fire Program .
RB	Used By Fire Program
RC	Pointer To ROM For Background Program
RO	Used By GSE Program
RE .	Used By Fire Program
R F	Used By Fire Program

TABLE 3-1 MEMORY LOCATION USEAGE

MEMORY LOCATION	IDENTITY	7	6	BIT ALLOCA	ATION 4	3	2	1	0
OC22	DMA Status Register	_	-	•	-	Rom Check Data	H' Data	Parity 1	Parity 2
OC23	Output Status Register	Time Share	GSE 1	Head Test	GSE 2	Inhibit	Fire	Fault	DMA Data
OC24	True Status Register					Inhibit	Fire	Fault	
OC25	Internal Plags Register	Button			Other Proce- ssor Dead	Rom Check	Head Test	Fault Button	Enter Fire Program
OC45	Port 3 Data	-	•	GSE 4 I/P	Fire Button	GSE 2 I/P	GSE 3 I/P	Fault Button	GSE 1 I/P

Registers are initialized for pointing to RAM memory locations specifically RO, the DMA pointer, R2, R5, RA and RF (lines 12-15).

At this point, program operation determines whether it is to run the fire program or under control of GSE. The hardware input, bit 5 of port 3 called GSE 4 INPUT, is set to a 'l' if GSE is disconnected and '0' if GSE is connected and active. Program steps at lines 18 to 20 determine the GSE status. If GSE program is to be run a jump to the separately described GSE program occurs.

A fire program will automatically occur if GSE is not connected.

Program then determines whether it has data retained in memory from a previous flight. To perform this, three locations are allocated to storage of an identity pattern. On start-up, all RAM locations will be in a random bit pattern if the battery is not holding RAM supply voltage up. By setting the three locations to a bit pattern, A5,A5,A5, the program can determine whether the memory should be reset.

If data has been retained from a previous fligh; and memory not read out (and subsequently reset) by the GSF then the pattern A5,A5,A5 will exist at locations OCO1, OCO2 and OCO3.

The program at lines 21 to 43 check for the A5,A5,A5 pattern, if confirmed the memory is not reset. If not confirmed, the program utilizes a subroutine RMTAR, lescribed in Section 3.2.4. to test and reset to zero all locations of the volatile memory (note that this reset function serves to reset the main timer at location OC26 and OC27). Subsequently, locations OC01 - OC03 are all set to contain bit pattern A5.

The initialization program then sets the H(OLD) location OCC7 to H'FF' indicating at this stage that all heads in the system are good. Subsequent head tests and fire program will then modify this location according to the aircraft configuration and number of heads utilized within that configuration.

Program lines 44 to 50 effect zeroing of memory locations referred to on the memory map as W,X,Y,Z,W',X',Y',P and P'. These locations are used by the fire program and are further described in Section 3.5.

The processor side now needs to know whether it is to act as a master or slave processor. The purpose of this hardware input is to enable software to set the operation of the two sides such that they are functioning in anti-phase, i.e. while say, side I is in the gather phase, side 2 will be in the process phase.

To input the hardware status of the master/slave bit, which is resident on DMA input ports, it is necessary to effect a

bootstrap DMA operation and then to run software checks on the input data. This operation is performed between lines 51 and 71 and is identical to that described in Section 3.5.1.1.

The configuration data of the DMA ports i then stored at location OCD7 and is called the configuration yte (lines 72 to 74).

For correct operation of its first pass it must appear to the fire program that DMA data has been received from the second processor. To effect this the low bits of memory locations OCDF to OCE6 must be set to 1,1,0,0,1,1,0 and 0 respectively. This is effected between lines 75 and 79.

At line 80 che program looks to see if the inhibit line into it has been flagged high by the second side. This operation is included here to eliminate the possibility of the return to a functional state of one side after its power lines have been interrupted. This is necessary because the system cannot reconfigure to a two sided system once one side has exhibited a fault condition. Therefore, if a system started with both sides functional, and then say side 2 failed due to a power supply interruption, side 1 would reconfigure to a single sided system and raise its inhibit flag line. In the unlikely event of side 2 being repowered while side 1 is still running, the software of lines 80 and 81 ensure that the side runs into a latching fault LACHFL routine, effectively running in a passive loop.

Timer constraints explained in Section 3.4.3.3. are then loaded to memory locations OC28,OC29, and OC2A (lines 87 to 89). This is followed by clearing memory locations OC20 to OC25, locations used by the gather phase of the interrupt program (lines 91 and 92).

Line 93 sets parity bits for transfer by DMA activity as discussed in Section 3.4.4.

3.2.2. Start up Timing

Assuming that the system is A type, it is necessary to ensure that both sides are synchronized in a manner so that one side will issue its time share high (allowing hardware to pass high voltage to the heads) and the second side will issue its time share low (such that its heads are off line). Subsequent timing of the two sides operation is then accomplished by the interrupt program.

What must be taken into account is the fact that both sides may differ slightly in the time taken to reach a given point in the program. This difference is a function of the tolerance of components associated with the "power-on reset" circuit and tolerance of the crystal and hence the system clock.

Program execution between lines 96 and 145 takes the above timing discrepancies into account, operation of which is as follows:

When program execution of say, side I reaches line 96 a hardware flag is output on the time share output line of port 4. This flag output is also directly connected as a flag input to the second side on its EF2 NOT) input. Conversely, the EF2 (NOT) flag input to side . signals the status of side 2 processors time share line.

Allowance is made for the possible delay of the second side reaching the point where it issues a flag 'l' level on its time share line. A time delay is built into the program, throughout which a check to see whether the EF2 (NOT) input has changed state. If the time delay times out (approximately 6 seconds later) before side 2 issued EF2 (NOT) = 1 then the second side is inhibited. Lines 98 and 99 load the delay constant to the timer and program jumps to line 110 to execute the delay. After each instruction the status of the EF2 (NOT) flag is checked. If it changes state the delay program is terminated by a jump to label HALF.

If the delay program times out it is presumed that the second side has failed to start (or that the system is type B). This results in the logging of an error code to a location reserved for codes which effect shut down of the second processor. The time of shut down is also logged. Locations used are OCIB and OCID.

Assume again that correct start up of both sides has occurred then the slower side, on entry to the time delay program, will immediately exit from same because the quicker side has issued a time share 'l' flag and is at this time executing a delay sequence. At the moment the slowest side issues a high time share output, synchronization has been achieved and both sides proceed to the next step by determining at line 103 whether they are master or slave. If the side is master, program jumps to label GO on line 128.

If the side is slave, the time share line must be reset to '0' i.e. heads off line (at line 107).

3.2.3. Further Housekeeping Requirements

Further housekeeping requirements for correct entry to the fire and interrupt programs must then occur. Line 108 sets R0 to OCFF, because subsequently the slave side goes directly (via the background program) to the fire program, this program expects to see OCFF in R0 as if a DMA transfer has taken place in the previous gather phase. Because at this time no prior gather phase has taken place for the slave side, it must be simulated. A flag is then set in the internal flags register, OC25 such that the fire program is immediately entered via the background program described in Section 3.3.

Program execution has now reached label GO at line 128. At this point the interrupt program counter Rl is loaded with the start address of the interrupt program (H'0606').

Register R2, the stack pointer, (described in Section 3.4) is initialized to point at stack memory location OC90 and R5 and R6 are initialized to suit the needs of the interrupt program.

It is necessary to process the configuration byte before entry to the fire program. This is effected by setting the address of the program ADJSET in R9 and then executing a subroutine call at line 136, the resultant parity checksum generated by ADJSET is stored at OCDA by line 137.

After enabling interrupts to occur (line 138) program control is passed to R3 and execution resumes via the background program.

3.2.4 Ram Test and Reset Routine

This subroutine is called by the initialization program and the GSE program. Its function is to perform a test on all random access memory locations and then to reset them all to zero.

Program listing is shown from line 146 of the initialization program.

Entry to the program is at line 149, all locations are checked by loading AA to each, followed by reading them back to the accumulator and executing a check to ensure that the write operation was correctly performed. This is repeated by writing 55 to each location. Failure to respond correctly to the test results in the loading of a fault identity and a jump to the LACHFL routine.

Following the above test all memory locations are reset to zero and the program control is returned to the calling program.

3.3. Background Program

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The background (or main) program performs a continuously cycling test on the content of the read only memory, thus ensuring that at all times, all program steps are correct. This is necessary particularly in the case of routines that are not flexed in the course of normal operation or when FIRE or FAULT buttons are pressed, for example LACHFL.

In effect this program is split into 12, 256 byte pages. Each page is checked individually by adding all bytes together, the resultant byte (ignoring all carries) is then compared with a checksum stored in a convenient area of the memory. Failure to check out correctly causes the side to shut itself down.

As a confidence check the second side allows a given time for the primary side to carry out the check (and vice versa). The second side, as part of the interrupt program, down counts a register. If the counter reaches zero before the primary side indicates (via DMA transfer) that the operation has been completed on all ROM a fault condition is issued by the second side and effects a shut down of the faulty side by issuing a high on its inhibit line.

The background program is functional only when head data is being gathered, i.e. when time share of the side is high, and the program operation allows only one page to be checked per gather phase.

Purther operation of the background program is to control the entry to the fire program.

3.3.1. Background Program Operation

On entry to the background from the initialization program, a register is set up pointing to RAM, this pointer is initially set to OCOO, i.e. 1 byte above the highest program bit (OBFF), this occurs on lines 0010 and 0013.

A memory location is assigned to act as an accumulator for ongoing result of the addition of each memory byte within the page being checked. This memory location is OC2C.

A check to determine whether time share is high or low is then carried out at lines 14 and 15, the check is carried out once, i.e. on entry to the background program from initialization and allows immediate transfer to the fire program if the side is slave.

The same check is then carried out at lines 17 and 18 as part of the cyclic operation of the program.

To ensure that only one page of memory is checked per gather phase the check at line 19 is included. The interrupt timer R5 (0) which counts down from H'C8' at the start of the gather phase, to H'13' at completion. Checking for the R5 (0) value being less than H'C0' gives a window of eight interrupt occurrences for the page check to be started. Because the page check will take more than eight interrupt periods, only one page is verified per gather phase.

The test at line 19, if passed, leads to the checking of a page of ROM. The accumulator at OC2C is then rezeroed. (line 22).

Program lines 23 to 26 get each ROM byte as pointed to by the pointer and adds them into the accumulator. At the completion of the page the resultant accumulator value is compared with the check sum values stored at memory locations 0800 to 0808.

Location 0800 points to page 0 checksum, up to location 080B which points to page B checksum. The fact that the lower byte value of the memory location is the same as the page number is utilized by the program to access the checksum value (line 28 and 29). Lines 30 and 31 execute the checksum comparison with the page accumulator, failure to compare correctly results in the loading of a fault identity and a jump to the LACHFL routine (line 48).

With the page correctly checked, the page pointer is initialized to the next page below or if zero page has just been checked, back to page B. (lines 32 to 36)

Program continues by returning to the label HELIUM by this time the interrupt counter is below H'CO' and no new page of program is checked. Instead program jumps to line 49 where it wants to see the occurrence of a flag which allows it to proceed to the fire program. This flag (bit O of OC25) is set by the interrupt program at the completion of the gather phase (line 146 of gather phase interrupt program). When the flag line is set, program proceeds at line 51 where parting bits of the DMA status register are loaded before passing program control to R7 which is the fire program pointer.

At the occurrence of subsequent gather phases the next page of ROM is checked as pointed to by the high byte of the ROM counter. When the check at line 34 indicates that all pages have been checked program jumps to line 38. A flag is set at bit 3 of the internal flags register at location 0C25 which is used as an indication that the ROM check has successfully been completed.

Program then repeats RAM checking from page B to page 0, in a continuous cycle.

3.4 Interrupt Program

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3.4.1 Interrupt Program Common to Gather and Process Phases

The interrupt program is responsible for timing of the two phases of operation, i.e.gather and process phases. The phases are so called because during gather, head data is being input to the system and during the process phase the received data is being processed by the fire program.

The interrupt program also performs logical operations on the head data as it is received and is also responsible for transfering data to the output port from the output register. This data is loaded to the output register at various points throughout the background and fire program, there will therefore in most cases be a finite delay (less than 832 microsecs) between an output state being requested and being executed.

The program is entered at line 72 of the gather phase listing of the interrupt program. Register R2 is pointing to a stack in memory such that on entry a new free area of stack is made available by operation at line 72. The T register (which contains the X and P pointer register values immediately after the interrupt event) is then saved in the stack, another free area is made available and the value of the accumulator (D) and the carry flag (DF) are also saved in the stack.

At lines 78 to 80 a memory location is pointed to which is to save the new state of the 8 heads available as input port 7. Memory location OC44 is the location used. Instruction on line 83 effects the storage of the head data.

The program next checks to determine whether the test flag is set. The test flag is set by the last interrupt of the process phase when it computes that 15 seconds has elapsed since the last head test. If this flag is set the effect of program lines 87 to 94 is to set the output port 4 with FIRE = 1, INHIBIT = 1, HEAD TEST = 1. This is copied from the output status register, however the true status register does not have FIRE = 1 and INHIBIT = 1 because the real condition is that a fire does not exist the output is only as a response to a test condition.

At this time the internal flags register is also copied to R4(1).

The head test output at '1' causes the emitters at the detectors to fire such that during this gather phase a large number of pulses is input to memory allowing the fire program to verify quality of heads.

The fire and inhibit line outputs at 'l' level allows the cutput relay to operate, in fact due to the speed of software operation, a signal at EF4(NOT)input will change state and be verified before the mechanical contact has time to change over. The result of verification is to immediately set inhibit and fire outputs back to zero.

Line 96 of the program checks to see whether the result of the output to fire and inhibit lines has resulted in the feedback check path to EF4(NOT) changing state.

If the change has occurred and the test flag was set it is reset and the fire and fault signals returned to zero (if a true fire was not existing at the time the test was performed). To verify this, reference is made to the true status register, operation of this conditional reset is documented between lines 183 and 198.

The EF4(NOT) line will also be indicating a fire condition at the output if a true fire exists or if the opposite processor is conducting a test on the output circuit, these conditions are tested between lines 172 and 182. If the conditions are met then

program operation continues at line 99, otherwise the EF4(NOT) line has been raised in response to a hardware circuit failure and the side is shut down by entering a fault code and branching to LACHFL.

If the condition at line 96 is such that no return signal at EF4 (NOT) has been received then this is conditional on whether a test had been initiated. If the test had not been initiated, then no high signal would be expected and program continues at line 99. If however a test had been initiated and no response has occurred, several reasons exist for this. They are that the fault output is set, and because in the hardware of the common logic card fault over rides fire, no return confirmation will occur. Or because the second sides inhibit line is raised. Failure to meet these conditins indicates that the lack of response to the test is a function of hardware failure and a fault is issued via the LACHPL routine. If the conditions are met operation contines at line 99.

At line 99 the interrupt timer, which controls the duration of the time share period is decremented.

At line 104 it is determined whether the time share line is high or low and program divides accordingly.

3.4.2 Gather Phase Program

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If at line 104 time share is low the gather phase program starting at line 107 is executed. The head data stored at OC44 is processed in the manner described in section 3 of Appendix A-1 such that the FOURS, TWOS and ONES COUNT is generated, this is peformed (lines 108 to 129) in such a way that when all three registers are full no overflow occurs.

FOURS, TWOS and ONES data is stored at locations OC40, OC41 and OC42.

The data so stored can represent up to a maximum of 7 counts in one gather phase, i.e. if bit 0 of each location is set to a 'l' the head 1 has gathered a minimum of 7 strikes in the gather phase. At each occurrence of the interrupt program during the gather phase the three locations are updated according to the latest data available from the heads.

On completion of the head data processing the program determines whether the gather phase is complete by looking at the count in the interrupt timer counter (line 131). If the count has reached D'13' then the number of interrupts since the start of the gather phase has been 200 (the interrupt counter was initially set to D'213'). As each interrupt is 832 microsecs apart it follows that the total length of the gather phase is 832 x 200 microsecs ie 166.4 ms.

If the count has not decremented to D^113^4 program returns to background operation.

If the gather phase is complete, operation determines firstly whether the completed phase was one where a head test was carried out, i.e. with emitter struck. The head test line of the output register is looked at (line 133 to 137) if high the last phase was a head test.

Program operation then verifies whether the emitter circuit has fired, this is carried out by observing the EP3 (NOT) status.

Two conditions then exist, if the head test was requested, the EF3 (NOT) line should give a positive verification, program execution jumps to line 148 and the EF3 (NOT) line is checked. If the verification shows that the emitters had not received a strike initiating voltage a fault code is loaded and a jump to the LACHFL routine occurs. This is necessary as the system would otherwise be unaware of the status of heads (lines 164 and 165). If the flag line shows that emitters do have a strike voltage applied, the head test line (and the GSE 2 line which mimics it) is reset at line 157.

A short delay of approximately 160 micro secs is then initiated at line 159. When this times out a further check is carried out to determine whether the emitters has cleared in response to line 157. The delay is necessary to ensure that head circuit capacitance does not influence the result of the test at line 161 where again the emitter voltage is examined. If for any reason (i.e. a hardware failure) the emitter voltage remains high a fault identity is loaded and a jump to the LACHFL routine occurs.

If no head test was requested during the last gather phase, program continues at line 138 at which the emitter line EF3(NOT) is checked. Program expects to find that the emitter line voltage is low, however if the flag indicates that it is high (due to a hardware failure) then a fault identity is loaded and a jump to the LACHFL routine occurs.

Program operation has now reached line 140 at which the interrupt timer is reloaded to a count of 213 ready for timing of the next process phase. The time share output (and GSE1 output which mimics it) is reset to zero such that the heads are taken off line ready for the process phase (lines 142 to 145).

Before returning to the background program, the fire program flag is set (bit 0 of memory location 0C25), this enables the background program to pass control to the fire program as explained in Section 3.3.

Exit from the interrupt program commences at line 66 where the statuses D, DF, and T are recalled from the stack and reloaded appropriately ready for the return to the program that was interrupted (at line 71).

3.4.3 Process Phase Program

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The process phase program starts at line 66 of the listing titled "Process Phase Interrupt Program"

The primary function of this program segment is to perform and monitor timing functions of the system. The program ensures that the duration of the process phase is correct and monitors the second side to ensure that it is effecting correct timing of the gather phase.

At line 66 the first check is to determine whether the second side is functional, this is executed by checking the internal flags register which has previously been duplicated to register 4.

3.4.3.1 Process Phase Operation for a Currently Fault Free System A

The program contines at line 70 and commences to carry out timing checks on the second sides time share output.

The gathering and processing sides will both be decrementing their respective interrupt times at the rate of one per interrupt event. When the gather side decrements to a count of 13, at which stage it changes its time share output from '1' to '0', the process phase interrupt timer should also contain approximately 13, errors will exist due to component tolerances. If the process phase timer decrements to zero before the gather phase time share changes from '1' to a '0' state, then the timing is sufficiently in error for the side acting in process mode to effect the shut down of the second side.

Program at line 70 checks to determine whether the interrupt timer has reached 0, if it has program jumps to line 192.

The internal flags register is checked to see if the second side is already inhibited, if not it up dates the register and loads an inhibit flag to the true status register (line 196). An error code is then loaded to the location (OClD) defining the reason for a second side shut down and the time at which the event took place is copied from the main timer counter to locations OClB and OClC (lines 197 to 203).

The output register at OC23 is then copied with an inhibit flag which is subsequently output to hardware at the next entry to the interrupt program (line 204 and 205). A jump to the program segment which is functional only at the completion of the process phase then occurs (Section 3.4.3.3.)

If the interrupt timer has not decremented to zero the time share status of the second side is checked to determine whether it has changed to a zero.

If a change of the second side from a gather to a process phase

is indicated, program continues at the segment which is functional at the completion of the process phase (section 3.4.3.3.)

If no change of the second side from gather to process is indicated, program continues by handing control to the DMA program explained in section 3.4.4.

On return from the DMA program the interrupt program is exited via the status restoration path explained in section 3.4.2.

3.4.3.2.Process Phase Operation for a Faulty System A or a System B

Operation in the process phase is identical for a faulty second side and a system B. In both cases at some time previously bit 4 of the internal flags register has been set high. The result of the test at line 68 is then to cause program to jump to line 188.

When one processor side is off (or not included as the system B case) timing control is effected by the good side. To perform this the interrupt timing register is checked to determine if the process phase is completed (line 189). Time out occurs similarly to the gather phase when the register has decremented to D'13'. If time out has not occurred, program control returns to the background program via the exit route which reinstates saved conditions. If the time out has occurred a jump at line 190 to line 75 is effected.

3.4.3.3 Program Operation at Completion of the Process Phase

After the last interrupt has occurred in the process phase, i.e. when the interrupt timer has decremented to D'13', program will be routed to the listing from line 75.

The first step is to set the time share output to a 'l' (and to set its mimic GSE l), this is performed between lines 75 and 80 where the new data is first copied to the output address register before being output to hardware.

The interrupt timer is then re-initialized to a count of 214 ready for the next gather phase.

Lines 83 to 96 process bit 3 of location OC25, the RAM check status bit. This bit will periodically be set to 'l' by the successful completion of all RAM memory locations. The bit is transferred, by masking, to bit 3 of the location involved in DMA transfer i.e. OC22. At the same time the flag at bit 3 of OC25 is reset such that another successful RAM check will re issue the flag.

Lines 98 to 100 then reset the head test and fault status bits of the output register to zero, new data is then copied in at the commencement of the next interrupt. The condition of the fault and fire buttons are then tested to determine if a test is requested. The button status' are input at line 103 and masked to eliminate unwanted data on this input port, the result is stored at R5 (1). The fault flag is then copied into the flags register and the output register. Operation (between lines 107 and 120) is such that if the button was previously depressed and is now clear the flag and output register condition is cleared.

Line 121 to 131 perform the same function for the fire button, the flags register and the output register is set or reset accordingly. However in this instance the fire button results in raising the head test bit of the output address register to a '1'. This in turn causes the emitters to be active on all subsequent gather phases while the fire button is being depressed. The result therefore is that a fire condition is initiated at the CWU as a result of the emitter stimulus. In this way a test of the system logic is performed.

In the case of the fault test the fault lamp being illuminated at the CWU is only a check on common logic hardware.

When the fire test button is pressed, the time of depression is logged in memory locations OCIE and OCIE by copying the main timer content. This is carried out such that GSE can compute event times with respect to the time that the fire test button is depressed. With the pilot directive that the absolute time of the fire test must be recorded during pre-flight checks, a method of relating events during flight to real time exists.

Line 143 then effects the output of fault line and head test line requirements according to the demands of the test buttons.

At line 144 the memory location which contains the ROM check timer is decremented and checked to determine whether it is zero. This function acts as a check on the second side and is a race against the successful completion of the ROM check. For example side 1 will perform a ROM check every 12 time share periods at the end of which a flag is DMA transferred to side 2 to state that the test has been completed. On receipt the fire program resets the ROM timer to a high value. If the timer times out before the next receipt a fault is indicated implying that side 1 has not completed the test in the time specified.

At line 149, if the ROM timer has decremented to zero, program jumps to line 209 where a check to determine whether the second side is already logged as faulty is carried out. If not lines 210 to 218 outputs an inhibit to the output and true status registers and stores a fault code and time of fault at locations OC18 to OC1D. If the fault condition is new or not, program continues at line 219 where the inhibit condition is stored in the output register for subsequent output at the next entry to the interrupt program.

A similar procedure to the ROM check race is used to check that the second side is performing a head test every 15 seconds.

The counter at location OE29 is decremented at the completion of the process phase. If it times out before the occurrence of the second side's head test a fault condition is initiated. When the second sides head test is performed the DMA status transmitted reflects this and the fire program re-initializes the counter (see Section 3.3.2.2)

Line 150 to 153 decrements the 16 second counter and checks for zero content. If the count is zero a jump to line 223 occurs. A check is carried out to determine if a fault has previously been initialized by this route, if not flags are set at bit 4 of the internal flags register and bit 3 of the true status register. An error code and time of error is then loaded to locations OClB to OClD (lines 226 - 234). At line 235, if the fault condition is new or not an inhibit bit is loaded to the output register.

Program next jumps to line 154 at which the timer responsible for setting a head test at 15 second periods is decremented. The timer (at location OC28) is then checked for zero content.

If the timer has timed out at line 158 the timer is reset to its initial value.

The main timer is then incremented at lines 158 to 166 taking into account the fact that the counter is two locations wide and incrementing the high byte if overflow from the low byte occurs.

Note that the main timer is incremented once every 15 seconds thus all data events are recorded against 15 second markers.

At lines 167 to 177, to prepare the next gather phase for a head test, bit 2 of the internal flags register, the head test bit is set. The output register head test bit and its mimic GSE 2 is also set to '1'.

The internal flags register test flag (bit 6) is then set to l at line 178 to 182. The new output register status is then output at line 184 causing hardware to pass a high voltage to the emitters.

At line 185 whether the 15 second period was completed or not, R6 is loaded with requirements of the DMA program (section 3.4.4.). The process phase is completed by returning to the background program via the exit routine at line 66 of the gather phase program where saved conditions are reinstated.

3.4.4 DMA Program

The DMA program takes data from memory locations OC20 and OC22 and transfers it out serially via bit 10 of the output port.

The required sequence of events is to set or reset bit '0' according to the data bit being transmitted. An output instruction to port 1 which acts as a clock pulse effects data latch into, and initiates DMA operation of the second side. The cycle repeats until all data is transmitted. Each data bit is transmitted twice, the two memory locations OC20 and OC22 are reset as the transmission occurs.

Only one DMA operation occurs on each event of the process phase of the interrupt program, since 16 data bits are transmitted twice, 32 interrupts occur after Q is set by the fire program before all data is transferred.

On entry to the DMA subroutine which occurs during each pass through the process phase, the status of the Q bit is first checked. DMA transfer will only occur if the Q bit is set, as dictated by the Fire program (section 3.5) if not set, control returns to the calling program.

Register R6, previously set at the last pass through the process phase to H'0110', is used to determine whether the data bit is being transmitted for the first or second time and to count the number of bits transmitted. Bit 'O' of R6(1) is at '1' if the bit being transmitted is first pass and at 'O' if second pass Bit 4 of R6(1) is used to indicate if both bytes have been transfered Because 16 transfers per data byte occurs, R6(0) is initially set at H '10' and is used to determine when all bits have been transfered twice.

When Q becomes set by the fire program, the DMA program which samples the Q line at each pass, through the process phase, proceeds to line 16. At this point R8 is set to be used as pointer to the output register and two locations from which data is to be output (OC23, OC22, and OC20 respectively).

At first entry, R6(1) bit O is at '1' and program continues at line 20 where R6(1) bit O is reset. At line 22 and 23 bit O, the data transfer port of the output register, is cleared to '0' and at lines 24 and 25 the low bit of location OC22 is copied to the output register.

Program steps 26 and 27 then output the data bit which is subsequently clocked into the second side by an output instruction to port 1. Decrementing R6(0) at line 28 indicates that one transfer of the current byte at OC22 has taken place. With R6(0) now at H 'OF' program jumps to the exit segment of the interrupt program.

On the next entry to the DMA program bit 'O' of R6(1) is now zero and from line 19 program jumps to line 42. At this point R6(1) bit 'O' is reset to 'l' and the data at OC22 is shifted such that the next bit for transfer is now resident at bit 'O' position.

The branch from line 46 to 26 now initiates the second transfer of the first bit which is still stored at bit 0 of the output port. Register R6 is decremented before exit from the interrupt program occurs.

At the third and fourth entry to the DMA program the second bit of location OC22 is output. This is repeated until all bits of OC22 have been transferred, at this time when the test at line 30 occurs R6 (0) is zero. A check at line 31 determines if both bytes have been transferred. If bit 4 of R6(1) is low as at this time it is set to a '1' along with bit '0' of R6 (1), R6(0) is re-initialized to enable the next 16 data transfers to be counted (lines 33 to 35).

The memory location now to be transferred serially out is OC20, this is first moved to OC22 from which the transfer will occur. (lines 36 and 37).

Subsequent entries to the DMA program cause the second data byte to be output in similar manner as the first until at line 30 the test again shows that R6(0) is zero. As this pass the test at line 32 shows that both data bytes have been output and program jumps to line 39, at which R6 is re-initialized and the Q output reset such that no further DMA activity can occur. The DMA program exit then occurs, and all subsequent entries cause no data transfer until the next fire program issues Q = 1.

3.5. Fire Program

The main function of the fire program is to process head data obtained from the last gather phase of the interrupt program resulting in the indication of fire or fault conditions.

Data may be fire data or data indicating the status of heads if the last gather phase was coincident with a head test.

The supplied data is processed as per the requirements of Volume I, Section 4.

The general method by which this data is processed is outlined in Appendix A-1.

Subordinate functions carried out by the fire program are:

- a) Recording the time at which a fire event occurred.
- b) Recording the adjacency area in which the fire condition occurred.
- c) Recording the time at which the fire reset occurred.

e) Recording how close the system comes to indicating a fire condition in terms of the number of successive gates filled by 4 or more pulses.

f) Recording the number of fire events.

Program listing for fire program is carried out in level 2 assembler a language peculiar to RCA. A summary of commands are contained in Appendix A-4.

Fire program listing is split into three segments named UNPACK, RENEW and FSET. These three programs call up three subroutines, ADJPR, ADJSET and HEADS.

3.5.1. Program Segment UNPACK

The program execution is dependant on whether the system is running as a System A or System B. (Note System A operation with a failed side is effectivley a System B)

Upon entry to the program access to the internal flags register at OC25 and detemines whether the second side is functional.

3.5.1.1. UNPACK With Both Sides Functional

If both sides are functioning correctly.

If data has been passed from the second side during the last gather phase then the register RO, used as the pointer for DMA data should be set to OCFF, this is checked by the program. If incorrect data has not been correctly received and a fault identity is loaded. Two reasons for this exist:

Firstly, due to some failure of the receiving processor, the second may have initiated an innibit. Program looks at the status of its EF1 (NOT) flag, if set (='1') then the second processor has initiated a side shut down. As a result a branch to the fault latch routine (LACHFL) occurs.

If EF1(NOT) = 0 no inhibit has occurred and due to failure to send data the second side is inhibited by jumping to program at NYOFF1. Program route in UNPACK is followed for a failed side and is discussed in Section 3.5.1.2.

At line 90, the data pointer (RO) is reset to OCDF ready to receive data at the next gather phase via DMA activity.

Program operation then checks that received data is via the two separate input channels of the logic card DMA circuitry. This it does by checking the port identity bit of the received data (referred to as X bit on flow diagram).

The check is carried out on memory locations OCDF and OCEO. Data at location OCDF should be as a result of one DMA port, data at OCEO should be as a result of the second DMA port. The hardware is wired such that the port identity bit is '0' at one input port and at 'l' on the second. The logic check at line 95 compares the two bits. If different, operation continues at label PS2. If incorrect a fault label is loaded and program executes a self shut down by LACHFL routine.

Further checks on received DMA data are carried out on the parity bits which are transmitted prior to any good data. Low bits of OCDF, OCEO, OCE1 and OCE2 should be 0,0,1,1 respectively. Lines 101 and 102 check for this compliance, failure causes program to pass to NYOFF1.

It is also essential to prove the hardwire linking configuration of the DMA ports which identify the adjacency set information to the program. It was essential to use two ports in the design such that verification could be achieved. This check is carried out at lines 105 to 111 by comparing memory locations OCDF and OCEO after inputed data and port identity has been masked off. The master/slave bit setting is also included in the check. Incorrect configuration results in a fault identity loading and jump to LACHFL routine.

Because of the need to include at the DMA ports a port identity bit it became necessary to eliminate one of the adjacency bits. Referring to the adjacency table of Section 9 of the report in Appendix A-1, it can be seen that by utilizing the 4th order bit only two adjacency set configurations are lost. However, it was evident that the set identified by llllllxx is desirable as this is the only case when a single headed system can be implemented. The second lost configuration identified by Olllllxx is effectivley duplicated by the configuration 110100xx.

Since without the fourth identity bit it is possible to identify the case IIIII as being unique, the program checks for this condition. To preserve the adjacency program written for 6 bits the 5 bit Jaha is converted to 6 bits before being stored to momenty location OCD7. Lines II3 to 120 check for the fourth order case and store the configuration data to the appropriate location.

The DMA received data from side 2, at locations of r to OCFE is only contained in the lowest order bit of ech byte. It is then necessary to unpack the status byte and the byte (H') containing either head data or the byte (W') containing the head test data. Note that the dash notation refers to the data received from the second microprocessor to distinguish it from that of the prime.

Lines 122 to 142 unpacks this data and reconfigures it to two single bytes. Unpacked data is stored at scratch pad locations OCB8 and OCB9.

3.5.1.2. UNPACK With One Side Paulty (Or System B operation)

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The jump to program label NYOFFL occurs due to a detected failure. Program at line 214 logs the status of the second processor at its internal flags register (bit 4 of OC25). Also true status and output status registers OC23 and OC24 are updated with inhibit flags set at bit 3 position.

Because program still requires the aircraft configuration data at the two DMA ports, it must "bootstrap" this information into memory. The hardware allows this to be effected by executing an OUT 2 instruction as described in Section 2.2.2.3.6. The configuration is inputed twice allowing delays such that data is transferred correctly (lines 221 to 224).

Program execution then checks for correct port identity, correct duplication of configuration bytes and checks for fourth order adjacency bit before storing the data, in similar manner to that of Section 3.3.1.1.

If correct data is not received from the second processor, the register containing W',X',Y', as described in Section 10 of Appendix A-1. must be set to Zero to ensure correct operation of the fire program. The H' register must also be set to an all faulty status. This operation is effected between lines 250 and 254.

Subroutine HEADS is then called. This processes received head condition data.

3.5.2. Program Segment RENE

The main function of this program segment is to update all registers associated with computation of fire conditions or all registers associated with head status dependant on whether the last gather phase gathered fire data or was a head test.

Program operation commences with a check on whether the second processor is successfully carrying out its own check on ROM content. The result of a successful check by the second processor is to initialize a flag bit in its status register which is subsequently transferred across by DMA activity. Lines 156 to 165 determine whether the status bit has previously been set by the second processor. If yes, the countdown ROM timer is preset to its initial count down value.

Further operation is dependant on whether received DMA data was W' or H' type. This is checked at lines 166 to 169 by observing bit 3 of the received status byte which is '0' if W' and '1' if H' gather function.

3.5.2.1. RENEW if W' Type Data

If the received data (now unpacked and resident at scratch pad location OCB8) is fire data, the registers W',X' and Y' must be updated. This operation is carried out after the jump from line 169 to NYOFF4 at line 196.

W' X' and Y' information is contained at location OCCC, OCCD and OCCE respectively. This data has to be shifted such that the last gather phase W' moves to X' etc. i.e. W' ---> X', X' ---> Y' and Y' is lost. This function is performed by lines 196 to 202.

3.5.2.2. RENEW if H' Type

If the received data was H' type, program continues at line 173. Firstly, it acknowledges the receipt of H' data by presetting the counter at OC29 to its initial down count value (line 174 to 176).

The H' data is then processed by the ADJPR subroutine described in Section 3.5.3.6.3. and then by subroutine HEADS.

At this point whether the system is A or B type all H' and W' data has been correctly processed according to the requirements of Appendix A-1.

Program action now concentrates on processing data from the last gather phase of its own side i.e. on W and H type data. NYOFF5 at line 262 is the point from which this is carried out.

Again dependant on whether data is W or H type two different routes are taken. The sides own internal flags register is interrogated to determine this at lines 263 to 264. The data about to be processed is that contained at the FOURS register location (OC40).

3.5.2.3. RELLW if W Types

The fire register F at OCD4 determines whether a fire is to be set. If a fire condition is existing, the fire indication remaining on is dependant on whether the new data received is such that at least two pulses per gate are being received as per the requirement stated in Volume I. Therefore, a fire condition for a head remains if the logic condition F AND 2's or 4s is satisfied. This result is stored for DMA transfer to the second side at location OC20 (to be received by side 2 as Winformation) and as Winformation.

Similarly, to W' data, W is processed by updating registers containing X,Y and Z data (as defined in Section 10 of Appendix A-1.)

Registers W, X,Y and Z are at locations OCCF, OCD1, OCD2 and OCD3 respectively.

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Data W moves to X etc., i.e. W-->X, X-->Y, Y-->2 and Z is lost.

The above processing is carried out at lines 327 to 340.

3.5.2.4. RENEW if H Type

If the last gather phase for its own side was a head test, H is processed according to program starting at line 277. Initially, a check is carried out to determine whether the new head status data H has differed from the previous H data (obtained 15 seconds previously).

The previous head status data is stored at location OCC7 and is termed HO. It determines whether a change of status has occurred when logic operation of lines 279 to 283 are performed. If the status has changed the new status is loaded to location OCC7 and the time of this change is logged at OCC5 and OCC6 by copying the main timer value to these registers. In this way the time of the last head failure can be identified.

The H data is also stored at OC20 for subsequent DMA transfer (see lines 290 and 291).

H data is subsequently processed by subroutines ADJPR and HEADS and ADJSET described in Sections 3.5.3.7.3., 3.5.3.7.2., and 3.5.3.7.1. according to lines 292 to 315.

The check sum figure generated through the ADJSET subroutine is then checked against the previously stored checksum at OCD2. If the new check sum differs according to lines 317 to 322 a fault code is generated and program jumps to LACHFL.

At the completion of the caps segment of the program a flag is set to allow the process phase of the interrrupt program to transfer data by DMA activity. The flag set is by raising the Q line output high and is performed at such a time that all data to be transferred has been loaded to locations OC20 and OC22.

3.5.3. Program Segment FSET

The main function of this section of the fire program is to calculate whether a fire condition should be set or reset according to all the data available.

Data logging functions are also performed.

Program FSET commences at line 356.

3.5.3.1. W COUNT Register

The initial operation performed by FSET is to update the memory location OCC3 and OCC4, termed the W count register. This register acts as a counter to store all occasions when a head has registered four or more head strikes in one time share period.

Each bit of the W register indicates if a particular head has received 4 or more strikes in the last gather phase. For each 'l' level in the W register the W COUNT register is incremented unless that is it is already full, (corresponding to approximately 65000 gates). This incrementing is only performed if the received data is not as a result of a head test.

Program implementation of the above is shown between lines 359 and 384.

3.5.3.2. Fire Level Logging

For a System A a fire condition is achieved when 6 consecutive gates (3 on each side of the system) are filled. A record is made of how near to this fire condition the system gets. For example, 5 consecutive gates may fulfil the fire condition but the 6th be clear. This is termed 5th fire level. The program treats the 6 gates W or Z,X,Y, and W',X' and Y' as a window, thus if say W,Y and X' were indicating filled gates (with 4 pulses) a 3rd level fire condition is registered.

When a fire level is detected the time that the event took place along with the head indicating the fire level is recorded.

This program is skipped if the current data being processed is as a result of a head test.

Memory locations OC51 to OC55 and OC66 are used as scratch registers for this program while locations OC56 to OC65 contain the stored data, according to the RAM memory chart, Figure 3-1.

This operation is fulfilled by program lines 386 to 444.

3.5.3.3. Calculations of Fire Conditions

Fire set and reset conditions are calculated from line 450 onwards. With reference to Section 10 of Appendix A-1., initially FL (termed in the software listing as the reset condition byte) is generated. Program lines 450 to 458 are responsible for this function.

Fire generation conditions according to the logic of Section 10 of Appendix A-1. are calculated between lines 462 and 502. This results in scratch pad register OCB8 containing all zeros if the fire is to be reset otherwise a fire condition is to be set or sustained.

3.5.3.4. Fire Condition Logging and Outputting to Hardware

If no fire condition is indicated the outputting program is skipped, When a fire condition is indicated by software the time and the adjacency set which caused the fire condition are logged. The program is arranged such that the occurence of the first fire and its start time is logged at locations OCCO, OCCl and OCC3.

The end of the event is recorded at locations OCBD, OCBE and OCBF. This procedure enables the duration of the fire event to be determined. To identify whether multiple fire events have taken place the memory location OCBC is used to store the number of fire events that have occurred. These operations above are carried out between lines 511 and 528 of the program.

The completed fire, or no fire, condition is then output to port 4 at line 535.

The fire condition is also saved at output status and true status memory locations.

3.5.3.5. Reverse Adjacency Processing

To enable the head data to be utilized in determining the next F register, the head data which has been adjacency procesed has to be unprocessed. This is performed as described in Section 11 of Appendix A-1.

The reverse adjacency processing is carried out between lines 547 and 564.

3.5.3.6. Housekeeping and DMA RAM Checks

At the completion of the fire program various resetting and checking operations are carried out between lines 576 and 589.

The FOURS, TWOS and ONES registers (memory locations OC40, OC41 and OC42) are reset to zero at lines 567 and 568. This is to enable correct operation of the next gather phase.

The memory locations OCDF to OCFE which receive DMA data, are also exercised to prove their correct operation. This is carried out by loading a pattern of H'AA' into each location and then checking that this write condition was successful. This is repeated with a pattern of H'55' to prove that each bit is capable of being set to 'l' or '0'. Failure to respond correctly to the tests results in the loading of a fault identification and a branch to LACHFL routine.

The DMA memory locations are then reset to zero and the DMA pointer register RO is set ready for the next DMA transfer.

Program operation then returns to the background program, pointed to by R3, at line 596.

3.5.3.7. Subroutines

3.5.3.7.1. ADJSET Subroutine

This subroutine is used to create the adjacency forms ADJ1, ADJ2, ADJ3 and ADJ4 as required by sections 5,6,7, and 8 of Appendix A-1. These forms are created from the configuration byte at locations OCD7 and stored at locations OCD8, OCD9, OCDA and OCDB.

A checksum generated through the program and is used to check that correct processing of the configuration data has been performed.

The ADJSET subroutine is shown between lines 602 and 668 of the fire program.

3.5.3.7.2. HEADS Subroutine

This subroutine is used to determine whether the number of heads in the system are sufficient to satisfy the adjacency set requirements. If a fire area has no ability to detect fire conditions the result of the computation (.NOT.H').AND.(.NOT.H) will be non zero. This non zero result is used to indicate a fault condition. This fault condition is copied to the true status register and output register. The fault is then copied to hardware by the next interrupt program. HEADS program is performed between lines 679 and 706.

3.5.3.7.3. Subroutine ADJPR

This subroutine is used to process the received head data W,W',H or H', condensing the individual head status into adjacency format. This is performed in accordance with Section 11 of Appendix A-1.

Program operation is performed between lines 714 and 735.

3.5.3.7.4. Subroutine LACHFL

This subroutine is called by the fire program and other programs of the system.

Its essential function is to shut down its own operation. Entry to the routine is performed with the accumulator containing the fault identity code of the function calling the LACHPL routine.

A list of codes generated before entry to the LACHPL routine are documented in Figure 3-3.

The routine saves this error code at location OCB5 along with the time (related to the main program timer) that the failure occurred at locations OCB3 and OCB4.

The interrupt routine is disabled on entry to the program.

Output code H'42' is passed to output port 4 before going into a loop, effectively stopping program operation. This output code raises the hardware GSE2 line high and issues a fault line high to the common logic circuit.

Program operation is performed between lines 747 and 768.

FAULT IDENTITIES

Self Shut Down Mode:

Identity	Description
01	No return path from o/p relay
02	Paulty common logic (alarm return permanently high)
03	No emitter operation (or return path)
04	Permanent emitter operation (or return path)
05	No emitter reset when reset by program
20	Error at RAM check
24	Bad DMA ROM check
25	Different Paths Check
28	No good paths
29 .	X bits of two DMA ports not different
30	Left configuration different from right configuration
A 7	Being inhibited by opposite side
Dl	Bad sum check byte
F9	X bits of two DMA ports not different
PP	Fault at ROM check.
Opposite sid	e shut down mode:
Identity	Description
80	Opposide side time share did not set at initilization
81	Opposite side time share time out incorrect
82	Opposite side not confirmed ROM check complete
83	Opposite side not confirmed 15 second head test

FIGURE 3-3 FAULT IDENTITIES

3.6 GSE Interface Program

The GSE program acts interactively with external ground support equipment which is detailed in a separate report.

The GSE program is entered if at start up the GSE 4 input line on port 3 is found to be at '1' at line 18 of the initialization program. The three GSE inputs, 1, 2 and 3 then determine which program is to be run. With three inputs eight programs are available.

Programs written in the system software are headed:

- 1) Td1.
- 2) Output Data
- 3) RAM Retention Part A
- 4) RAM Retention Part B
- 5) Common Logic Check
- 6) ROM Test
- 7) ROM Test and Reset
- 8) Board Test Routine

On entry to the GSE program the status of port 3 is input and all unwanted bits masked off such that only the three inputs, GSE 1, 2 and 3 are remaining (lines 15 to 17). A series of tests between lines 18 and 26 then determine which test is to be run according to the setting of GSE inputs 1, 2 and 3.

Completion of each test requested of the CCU results is confirmation by appropriately setting the GSE 1 and 2 output lines. This enables the connected ground support equipment to determine if the test has been passed or failed.

3.6.1 Idle Program

The idle routine has no specific function to perform, it is merely a convenient state to leave the system in when no function is being performed. Program operation starts at line 27. At line 28 the GSE 1 and 2 output lines are both set high by an output instruction. Program then runs into a loop at line 29.

3.6.2 Output Data Program

This program is responsible for transmitting out the contents of the RAM memory for analysis by the GSE. All memory locations are transmitted in ASC11 format at a rate of 300 baud.

The program from line 61 uses two subroutines, a delay routine called DELAY and a routine called out which outputs ASCII characters via the Q line which acts as the serial output port.

Register 6 acts as a points/ to RAM memory from which data is to be output. This is initialized to OCOO at lines 61 to 65. Start addresses of the two subroutines are then loaded to registers 8 and 9 at lines 67 to 70.

The computer card in the ground support equipment expects to see a string of characters which define where the following data is to be loaded. The string !M4400 is a statement that the memory contents of the CCU are to be stored from a starting address of 4400.

Lines 71 to 79 load sequentially the above string in ASC11 equivalent, by executing the OUT subroutine the character is transmitted on the Q line.

Lines 80 to 82 cause a space character to be transmitted 24 times, this causes the printer of the GSE to be set correctly to print the data as it is transmitted simultaneous with its storage to memory.

Program between lines 83 and 107 cause each CCU RAM memory byte, starting as address OC00, to be converted into ASC11 format and transmitted.

A carriage return character is then transmitted, this is recognized by the GSE computer card as the conclusion of data transfer.

The GSE 1 line is raised to a '1' indicating that the program sequence has been completed (line 111) and a loop function is executed at line 112.

3.6.2.1 Subroutines of Data Program

The ASCII characters, output at 300 baud, consist of a high level start bit, 7 data bits, an even parity bit and two stop bits. This requires that each bit be held high or low on the Q line for 3ms. The delay subroutine at lines 144 to 148 executes a 3ms delay before returning to the calling program.

On entry to the OUT subroutine, at line 115, registers are initialized R3(0) acts as a bit counter. The Q line is set for 3ms, this is the start bit. At line 121 a check is carried out to determine if all data bits of the ASC11 character have been transmitted. If not, the next bit is shifted into the carry register (lines 122 to 124) and dependant on the bit being 'O' or '1' the Q output is reset or set and the 3ms delay activated. Note that at line 126, register 1 is incremented if the next data bit is a '1'. This register acts to accumulate of the number of '1's' transmitted.

When the test at line 121 determines that all bits have been transmitted program jumps to line 131, at which Rl is used to recall if an odd or even number of 'l's have been transmitted (lines 131 to 133).

If even the Q line is set, if odd, the Q line is reset and the 3ms delay is initiated, thus performing parity transmission. Two stop bits (zero's) are then transmitted by resetting Q and executing two 3ms delays (lines 138 to 140).

Control then returns to the calling program.

3.6.3 RAM Retention Program (Part A)

This program is designed to run in conjunction with Part B (Section 3.6.4). Its function is to set up a data pattern in memory which is checked by Part B. The mode of use is to set the data pattern and subsequently switch system power off. On power up Part B then checks if the data pattern has correctly been saved by the battery back up and its associated control hardware.

Part A serves to set the data pattern H'00' at location OCOO H'01' at location OCO1 etc. up to H'FF' at location OCFF.

Program execution starts at line 30 and is completed by setting GSE 1 output to a '1' level at line 35 before entering a loop at line 36.

3.6.4 RAM Retention Program (Part B)

This program serves to check the bit pattern set in memory by Part A (Section 3.6.3). It does so by adding all memory location contents together (disregarding overflow) the resultant figure is then checked against a checksum.

Program execution starts at line 37. Lines 40 to 42 get and add all memory data bytes together storing the accumulated figure at R6(0). When all bytes have been added, the result is compared with the checksum at line 44.

If the check is good (i.e. the memory pattern is the same as that set by the program of section 3.6.3) both GSE 1 and 2 output lines are set to '1' before a loop is executed at line 48.

If the check shows an error, only the GSE 1 output line is set to a '1' (line 49) before a loop is executed.

3.6.5 Common Logic Program

The common logic program acts in conjunction with the ground support equipment to test the logic block of the common logic card. The test is designed to flex the fire and inhibit lines

individually such that it can be proved that in normal operation a fire condition is only indicated when both sides set their respective outputs. The output conditions on GSE 1 and 2 lines enable GSE to determine what part of the common logic program is being executed.

At program entry, a bootstrap operation on the DMA port is carried out to access the master/slave bit. At line 10, if the side is slave, execution of a 2 second delay occurs at lines 21 and 22.

If the side is master, the following sequence of events takes

If the side is master, the following sequence of events takes place.

- 1) Issue a time share, fire and GSE 2 output to port 4 (line 11) and execute a delay for 400ms (lines 12 and 13).
- 2) Reset fire and GSE 2 outputs and set inhibit and GSE 1 outputs (line 14) and execute a 400 ms time dealy (lines 16 and 17).
- 3) Reset inhibit and time share lines, and set GSE l and 2 outputs (line 18) then execute a loop at line 19.

If the side was slave, after the completion of the two second time delay (line 23) the master sides time share t is repeatedly sampled until it is reset after execution of the above steps (lines 22 and 23). When this occurs the slave side also executes the sequence of steps 1, 2 and 3.

3.6.6 ROM Check Program

The ROM check program is that run in the backgound program, as described in section 3.3.

The ROM check set up program sets data correctly for entry into the background program. The time share bit of the output register must be set to a 'l' (line 30 and 31) because the background program will only execute ROM check if the phase is gather. Furthermore it will only carry out ROM check if if the interrupt timer R5(0) has a count above H'CO', therefore line 32 stores H'FF' to R5(0). Entry to the background program occurs at line 35.

3.6.7 Board Test Program

The board test program listed from line 150 of the GSE program is used to fault find boards and does not interact with the ground support equipment or the normal operation of the CCU.

4.0 TESTING

4.1 Functional Tests

Functional testing of the component parts of the system was carried out in accordance with the following Graviner Quality Control Data Sheets, which form Appendix No. B-1 to this report.

Detector Unit Types 53522-011 and 50001-012

Q. Data Sheet No. Q.5304. Issue A

Paragraphs 5.2., 5.2.1., 5.3., 5.4.1., 5.4.2. and 5.5.

Applicable limits, Type 3 as paragraph 5.6. of 0.5304, appropriate at and between the declared extremes of operating temperatures.

Crew Warning Unit Type 53813-202

Q. Data Sheet No. Q.5308 Issue C

Paragraphs 4.3.2, 4.3.3, 4.3.4, 4.3.5, 4.3.6, 4.3.7, 4.3.8, 4.3.9 and 4.8.

Applicable limits. Type 3 as paragraph 8 of Q.5308, appropriate at and between the delcared extremes of operating temperature.

System A. Control Unit Type 53813-203

Q. Data Sheet No. Q. 5309 Issue A

Paragraphs 4.1, 4.2.1, 4.2.2, 4.4, 4.5, 4.7.3, 4.7.4, 4.7.5, 4.7.6, 4.8.3.1, 4.8.3.2, 4.8.6.2, 4.8.6.3, 4.8.9, 4.8.10, 4.9.2, 4.9.3, 4.9.4, 4.9.5, 4.10.2, 4.10.3, 4.10.4, 4.10.5, 4.11.3.2, 4.11.3.3, 4.11.3.5, 4.11.6, 4.11.7.1, 4.12.10.2 and 4.12.10.3.

Applicable limits, Type 3 as Appendix 1 of Q.5309, appropriate at and between the declared extremes of operating temperature.

System B. Control Unit Type 53813-204

C. Data Sheet No. 0.5310 Issue A

Paragraphs 4.1, 4.2.1, 4.2.2, 4.4, 4.5, 4.7.3, 4.7.4, 4.8.3.1, 4.8.6.2, 4.8.6.3, 4.2.8, 4.8.4, 4.9.2, 4.9.3, 4.10.2, 4.10.3, 4.10.4, 4.10.5, 4.11 1. 4.11.6, 4.11.7.1, 4.12.6.2 and 4.12.6.3.

Applicable limits, Type 3 as Appendix 1 of Q.5310, appropriate at and between the declared extremes of operating temperature.

4.2 Qualification Test Plan

The Qualification Test Plan is incorporated as ATS No. 52, Issue 5 which forms Appendix B-2 to this report.

A separate test plan has been formulated for Electromagnetic Interference with is incorporated as Appendix B-3 to this report.

4.3 Qualification Tests

4.3.1 Samples for Test

The following samples were supplied for testing:

Crew Warning Unit Type 53813-202 Serial Nos. 100 and 101

Computer Control Unit Type 53813-203 Serial Nos. 100 and 101

Computer Control Unit Type 53813-204 Serial Nos. 100 and 101

Dual U.V. Detectors Type 53522-011 Serial Nos XP1, XP2, XP6 and XP7

Single U.V. Detector Type 53521-012 Serial Nos. ENV, XP1, XP2 and XP5.

4.3.2 Approval Tests

The following tests only, of ATS No. 52 were carried out:

4.3.2.1 Weight (ATS 52 Para. 4.1.1)

The weights of a representative sample of components submitted for approval testing were checked and recorded as follows:

C.W.U. Type 53813-202 S/No. 100 0.581 Kg. C.C.U. Type 5381 -203 S/No. 101 3.699 Kg. Detector Type 535^2-011 S/No. XP2 0.142 Kg. S/No. ZP7 0.156 Kg. Detector Type 53521-012 S/No. XP2 0.099 Kg.

4.3.2.2 <u>Size</u> (ATS 52 Para, 4.1.2)

The dimension of all samples submitted for approval testing was checked a_{ℓ} of the relevant drawings and were found to be satisfactory.

4.5.2.3 Visual Examination (ATS 52 Para, 4.1.3)

All samples submitted for approval testing were examined for correctness of marking, workmanship, visible defects, and were found to be satisfactory.

4.3.2.4 Center of Gravity (ATS 52 Para. 4.1.4)

The center of Gravity of the following items of equipment was established using the knife edge method and is shown in Figure Nos. 4-1, 4-2, 4-3, 4-4, and 4-5.

C.W.U. Type 53813-202	S/No. 101
C.C.U. Type 53813-203	S/No. 100
C.C.U. Type 53813-204	S/No. 100
Detector Type 53522-011	S/No. XP6
Detector Type 53521-012	S/No. XP1

4.3.2.5 Voltage Supplies (ATS 52 Para. 4.2.1)

The component parts of the system were operated from power supplies in accordance with MIL-STD 704A, Equipment Category B, Emergency supply condition.

A.C. Voltage Limits

1

102 volts 380 Hz to 124 volts 420 Hz

D.C. Voltage Limits

16 to 29 volts

4.3.2.6 Voltage Transients (ATS 52 Para. 4.2.1)

The effect of the following voltage transients on the system has been established.

Voltage	Duration
190	0.10 second
174	0.40 second
139	4.00 seconds
137	5.00 seconds

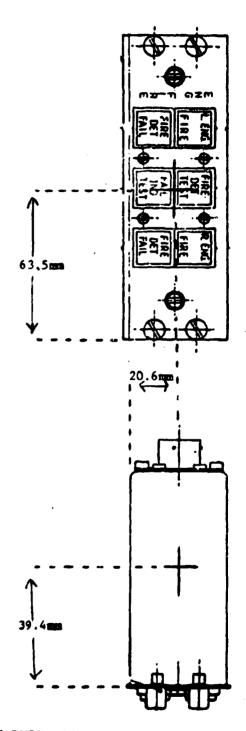


FIGURE 4-1 CREW WARNING UNIT TYPE 53813-202 CENTER OF GRAVITY

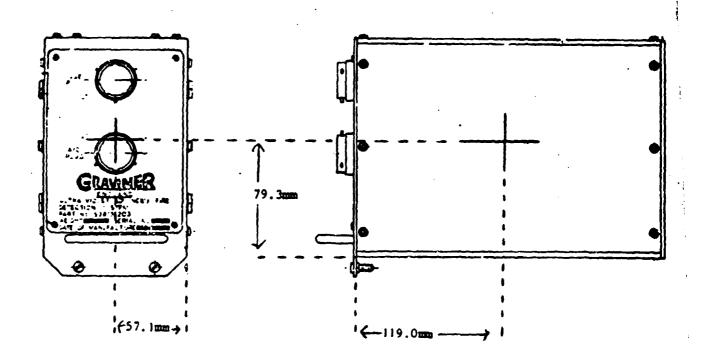


FIGURE 4-2 SYSTEM A CONTROL UNIT TYPE 53813-203 CENTER OF GRAVITY

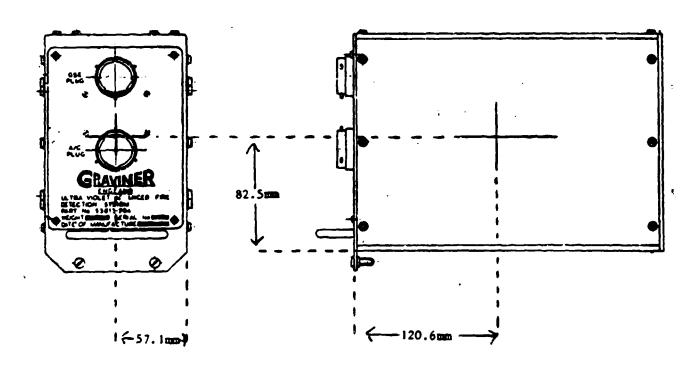


FIGURE 4-3 SYSTEM B CONTROL UNIT TYPE 53813-204 CENTER OF GRAVITY

FIGURE 4-4 DETECTOR UNIT TYPE 53522-011 CENTER OF GRAVITY

 $N_{\mathbf{q}}$

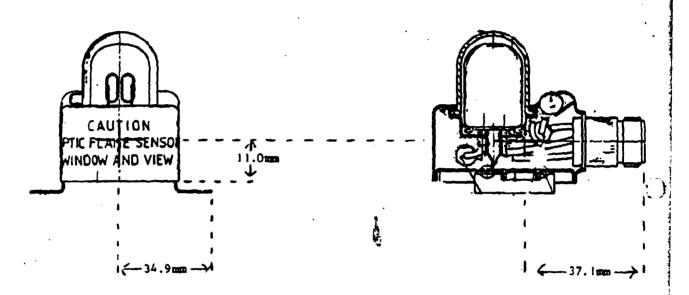


FIGURE 4-5 DETECTOR TYPE 53522-012 CENTER OF GRAVITY

Testing was carried out in accordance with MIL-STD-704A and the results of the tests are recorded in Lucas Aerospace Report No. LM80876. Appendix 5 (AED.ENV.480550) which forms Appendix B-3 to this report.

4.3.2.7 Supply Interruption (ATS 52 Para. 4.2.1)

The effect of Supply Interruption to the system has been established. Testing was carried out in accordance with MIL-STD-704A and the results of the tests are recorded in Lucas Aerospace Report LM 80876 Appendix B-3 (AED.ENV 480550).

4.3.2.8 Insulation Resistance (ATS 52 Para. 4.2.2)

Insulation Resistance Tests were carried out where necessary during approval testing as follows:

C.C.U. 30 volts d.c. between all unearthed terminal pin and case. (Leakage current not to exceed 1.5 uA)

The insulation resistance measured at all times exceeded 20 Megohms.

C.W.U. 500 volts d.c. between all unearthed terminal pins and case.

The insulation resistance measured at all times exceeded 20 Megohms.

Detector Unit. 500 volts d.c. between all unearthed terminal pins and case.

The insulation resistance measured at all times exceeded 20 Megohms.

4.3.2.9 Electromagnetic Interference (ATS 52 Para, 4.2.3)

The system has been tested to comply with the Electromagnetic Interference requirements of MIL-STD-461.

This work was carried out by Lucas Aerospace and the results of the tests are recorded in Lucas Aerospace Report No. LM 80876 which forms Appendix B-3 to this report.

4.3.2.10 Chattering Relay Test

The following test was carried out as a requirement of General Dynamics, using the following equipment:

System 'A' C.C.U. Type 53813-203 Serial No. 100 System 'B' C.C.U. Type 53813-204 Serial No. 100 C.W.U. Type 53813-207 Serial No. 100

and using the test configuration as shown on Figure 4-6.

Transient Impulse Susceptibility

No change in indications, malfunctions or degradation of performance shall be indicated in any equipment and/or its load when exposed to an impulse type electromagnetic field generated by a type MS25271 (or an acceptable equivalent) when wired for continuous operation with a switch in series with the positive side of the line from a 28V D.C. power source. No. suppression components (shielding, diodes etc.) shall be attached to the relay or its wiring. The unshielded positive lead leaving the switch shall be laid over three side of the test sample and then connected to the relay. The unshielded return lead from the relay shall be taped to, and in parallel with, input power leads, signal leads and interconnecting leads. The total length of each external wiring harness paralleled with the relay circuit shall not be less than 60 inches. The 28V input shall be reversed and the test repeated.

Equipment Used

System cableform as used for EMC testing refer to EMC report for details. Cableform wiring as per drawing Z22004.

Relay Type (NATO Stock No. 5945 92 192) Elliot HF 1201 C00

Control Unit System A (53813-203) Serial No. 100 Control Unit System B (53813-204) Serial No. 100 Crew Warning Unit (53813-202) Serial No. 100

Test Performed

The equipment was arranged as per Test set up and relay wiring diagrams.

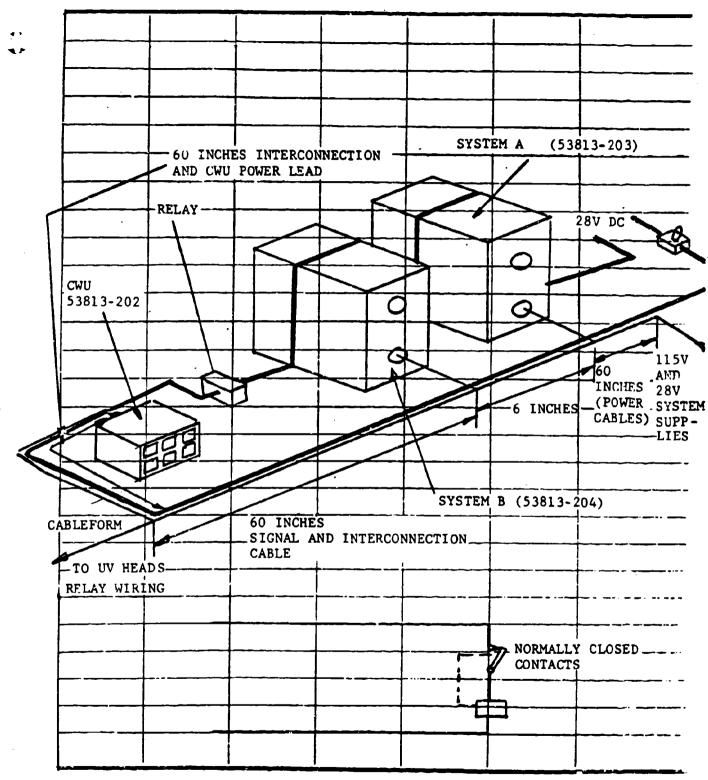


FIGURE 4-6 CHATTERING RELAY TEST SET-UP

With the system power switched on the control units were observed to function as per respective Q data sheets paragraphs 4.3.1 and 4.3.2.

The chattering relay supply was switched on and again paragraphs 4.3.1 and 4.3.2 of Q data sheet were carried out, namely

- (1) Depression of fire push button and observing that both L.ENG and R.ENG fire lamps operated correctly.
- (2) Depression of FAIL IND Test button on C.W.U. and observing that FIRE DETECT FAIL lamps functioned correctly. Correct operation of GSE1 and GSE2 lids on GSE control unit was also observed.

At no time during the test did the system show false indications, malfunction or become degraded.

The chattering relay supply was then switched off, the 28V supply reversed and the test repeated. Again no false indication, malfunction or degradation of the system was observed.

Conclusion

The system passed the chattering relay test.

4.3.2.11 Response and Reset Time (ATS 52 Paras. 4.3.2 and 4.3.3)

System 'A' comprising, C.C.U. Type 53813-203, S/No. 100, C.W.U. Type 53813-202, S/No. 101 and Dual Detector Type 53522-011, S/No. XP6 was subjected to Response and Reset Time test as follows:

The response time of the system was measured when the detector was exposed to a U.V. source at a distance of four feet.

The reset time of the system was measured when the U.V. source was removed from the view of the detector.

Exposure	Response Time	Reset Time
1	1.23 seconds	0.84 second
2	1.25 seconds	0.85 second
3	1.28 seconds	0.95 second

System 'B' comprising C.C.U. Type 53813-204, S/No. 100, C.W.U. Type 53813-202, S/No. 101 and Single Detector Type 53521-012, S/No. ENV was subjected to the response and reset time tests as previously described with the following results:

Exposure	Response Time	Reset Time
1	1.12 seconds	0.79 second
2	1.01 seconds	0.86 second
3	1.14 seconds	0.87 second

4.3.2.12 High Temperature (ATS 52 Para. 4.4.1)

System 'A' comprising C.C.U. Type 53813-203, S/No. 101, C.W.U. Type 53813-202, S/No. 100 and Fuel Detector Type 53522-011 fitted with fly leads (No Serial Number) was subjected to the high temperature requirements of MIL-STD-810C, Method 501.1, Procedure 1 modified as follows:

Detector - 24 hours exposure to 260°C C.W.U. - 48 hours exposure to 71°C C.C.U. - Not tested.

System response and reset with the detector at $260\,^{\rm O}{\rm C}$ was as follows:

Exposure	Response Time	Reset Time
1	1.35 seconds	0.952 second
2	1.15 seconds	0.832 second
3	1.26 seconds	0.911 second

The results of functional tests conducted on the C.W.U. at 71° C are recorded in Table No. 1.

System 'B' comprising C.C.U. Type 53813-204, S/No. 101, C.W.U. Type 53813-202, S.'No. 100 and Single Detector Type 53521-012 fitted with fly leads (No Serial Number) was subjected to the high temperature requirements of MIL-STD-810C, Method 501.1, Procedure 1 modified as follows:

Detector - 24 hours exposure to 260°C C.W.U. - As previously tested

C.C.U. - Not tested.

System response and reset with the detector at 260°C was as follows:

Exposure	Response Time	Reset Time
1	1.24 seconds	0.928 second
2	1.06 seconds	0.878 second
3	1.08 seconds	0.870 second

4.3.2.13 Low Temperature (ATS 52 Para. 4.4.2)

System 'A' comprising C.C.U. Type 53813-203, S/No.101, C.W.U. Type 53813-202, S/No. 101 and Dual Detector Type 53522-011, S/No. XP6 was subjected to the low temperature requirements of MIL-STD-£10C, Method 502.1, Procedure 1 and was exposed to a temperature of -54° C for a period of 24 hours.

System response and reset at -54°C was as follows:

Exposure	Response Time	Reset Time
1	1.804 seconds	0.907 second
2	1.253 seconds	0.908 second
3	1.183 seconds	0.939 second

The results of functional tests carried out on the C.W.U. and the C.C.U. at -54° C are recorded in Table Nos. 2 and 3 respectively.

System 'B' comprising C.C.U. Type 53813-204, S/No. 101, C.W.U. Type 53813-202, S/No. 101 and Single Detector Type 53521-012, S/No. ENV was subjected to the low temperature requirements of MIL-STD-810C, Method 502.1, Procedure 1 and was exposed to a temperature of $-54^{\circ}\mathrm{C}$ for a period of 24 hours.

System response and reset at -54°C was as follows:

Exposure	Response Time	Reset Time
1	0.842 second	0.774 second
2	0.861 second	0.752 second
3	0.494 second	0.879 second

The results of functional tests carried out on the C.C.U. at -54°C are recorded in Table No. 4.

4.3.2.14 Altitude (ATS 52 Para. 4.4.4)

Dual Detector Type 53522-011, Serial No. XP6 and Single Detector Type 53521-012, Serial No. ENV were subjected to the altitude requirements of MIL-STD-810C, Method 500.1, Procedure 1 and was exposed to altitude pressures equivalent to 70,000 feet (1.33 in Hg) and -1000 feet (30.12 in Hg) for periods of 1 hours each.

Throughout the test the detectors were connected to their respective C.C.U. and C.W.U.

System response and reset times after the altitude test were as follows:

Detector Type 53522-011, S/No. XP6

Exposure	Response Time	Reset Time
1	1.26 seconds	0.843 second
2	1.27 seconds	0.932 second
3	1.26 seconds	0.791 second

Detector Type 53521-012, S/No. ENV

Exposure	Response Time	Reset Time
1	0.95 second	0.826 second
2	0.89 second	0.724 second
3	0.93 second	0.664 second

4.3.2.15 Acceleration (ATS 52 Para. 4.4.10)

System A, C.C.U. Type 53813-203, Serial No. 100 and System B, C.C.U. Type 53813-204 (with battery card), S/No. 100. C.W.U. Type 53813-202, S/No. 101, Detector Type 53522-011, S/No. XP6 and Detector Type 53521-012,S/No. ENV were subjected to the acceleration requirements of MIL-STD-810C, Method 513.2, Procedure 1.

Acceleration levels of 25.5g were applied in each of three mutually perpendicular planes, in both forward and reverse directions and were held for a period of 60 seconds in each direction.

On completion of acceleration testing functional tests were conducted in accordance with the relevant Q.data sheet, the results of which are recorded in Tables No.s 5, 6, 7 and 8 (Appendix B-6).

4.3.2.16 Vibration (ATS 52 Para. 4.4.13)

The following items of equipment were subejcted to the following vibration tests:

Crew Warning Unit

Crew Warning Unit Type 53813-202, Serial No. 101 was subejected to a resonance search in accordance with Specification MIL-STD-810C; Method 514.2-2, Procedure 1; Curve J of Figure 514.2-2 and to random vibration in accordance with Specification MIL-STD-810C; Method 514.2, Procedure 1A; Figures 514-2-11A and 514-2-2A.

Computer Control Unit

The units, Computer Comtrol Unit Type 53813-203, Serial No. 100 (System A); Type 53813-204; Serial No. 100 (System B with Battery Card), were subjected to a resonance search in accordance with Specification MIL-STD-810C, Method 514.2.2, Procedure 1, Curve J of Figure 514.2.2; to random vibration in accordance with Specification MIL-STD-810C, Method 515.2, Procedure 1A, Figures 515-2-11A and 514-2-2A.

Detector Units

Detector Unit Type 53522-011, Serial No. XP6 and Detector Unit Type 53521-012, Serial No. ENV were subjected to a resonance search in accordance with MIL-STD-810C, Method 514.2, Procedure 1, Curve G of Figure 514.2-2 and to random vibration in accordance with MIL-STD-810C, Method 514.2, Procedure 1A, Figures 514.2-11A and 514.2-2A.

All items of equipment functioned satisfactorily during and after vibration testing and the results of functional tests are recorded in Table Nos. 9-20 inclusive (Appendix B-6).

This test work was carried out by E.M.I. Electronics Limited, Feltham, Middlesex, and the details of the vibration tests, including equipment axes, frequency ranges, vibration levels, resonance search results, are fully reported in E.M.I. report No. ENV 2739 which forms Appendix B-4 to this report.

4.3.2.17 Acoustic Vibration (ATS 52 Para. 4.4.14)

X

Dual Detectors Type 53522-011, 8/Nos. XP1 and XP7, Single Detector Type 53521-012, S/Nos. XP1 and XP5 were subjected to the acoustic vibration requirements of MIL-STD-810C, Method 515.2, Procedure 1.

The units were exposed to an overall sound pressure level of 154 dB measured using three Bruel and Kjaer Type 4135 microphones for a period of 30 minutes.

Functional tests were carried out before and after testing and the results are recorded in Table No. 21 (Appendix B-6).

This test work was carried out by British Aerospace, Dynamics Group, Hatfield, Hertfordshire.

Report No. ETR 2297, Test House Certificate A.W. 117 which forms Appendix B-5 to this report.

4.3.2.18 Mechanical Shock (ATS 52 Para. 4.4.12)

C.W.U. Type 53813-202, S/No. 101; System A. C.C.U. Type 53813-203, S/No. 100; System B C.C.U. Type 53813-204, S/No. 100 Detector Unit Type 53522-011, S/No. XP6 and Detector Unit Type 53521-012, S/No. ENV; were subjected to the mechanical shock requirements of MIL-STD-810C, Method 516.2, Procedure 1.

Each item of equipment was subjected to a total of 18 shock pulses of 20.0g for a duration of 11.0 milliseconds. Three (3) shocks in each of 3 mutually perpendicular planes in both forward and reverse directions.

Functional tests were carried out after shock testing and the results are recorded in Table Nos. 22, 23, 24 and 25 (Appendix B-6).

4.3.2.19 Flame Sensitivity (ATS 52 Paras. 4.3.2 and 4.3.3)

System A, comprising C.W.U. Type 53813-202, Serial No. 100; C.C.U. Type 53813-203, Serial No. 100 and Dual Detector Type 53522-011 without Serial number fitted with fly leads was subjected to the flame sensitivity test as follows:

The detector unit was exposed to the radiation from a 5" diameter pan fire containing JP-4 aviation fuel at a distance of 4 feet.

The system indicated "Fire" after exposure to the flame. The "Fire" indication continued when half of the flame radiation was blocked from view of the detector and the system indicated "Fire Out" upon removal of the fire radiation source.

System response and reset times were measured at the system supply voltage extremes with the following results.

System A

System Supply	16.0v D.C.	=	Ov D.C.
Voltages	102v. 380Hz		v 420 Hz
Response	Reset	Response	Reset
Time	T i me	Time	Time
1.31 seconds	0.80 second	1.256 seconds	1.41 seconds
1.50 seconds	1.04 seconds	1.117 seconds	0.90 second
1.23 seconds	1.57 seconds	1.111 seconds	1.0 second

System B, comprising C.W.U. Type 53813-202, Serial No. 100; C.C.U. Type 53813-204, Serial No. 100 and Detector Unit Type 53521-012 with Serial number fitted with fly leads, was subjected to the flame sensitivity test as previously described with the following results:

System B

System Supply 16.0v D.C.		29.0v D.C.	
Voltages 102v 380 Hz		124v 420 Hz	
Response	Reset	Response	Reset
Time	Time	Time	Time
0.764 second	0.821 second	0.986 second	0.715 second
0.836 second		0.910 second	0.654 second
0.856 second		0.876 second	0.751 second

4.3.2.20 Exposure to Flame (ATS 52 Para. 4.5.3)

System A, comprising C.W.U. Type 53813-202, Serial No. 100; C.C.U. Type 53813-203, Serial No. 100; Detector Unit Type 53522-011, Serial No. XP7; Detector Unit Type 53522-011 without Serial number and filled with fly leads, was subjected to the "Exposure to Flame Test" as follows:

The detector without serial number and 6" of wiring was immersed in a $6" \times 1100$ °C Flame.

Detector Serial No. XP7 was positioned so as to detect the flame but was not immersed in it.

The 6" \times 1100°C Flame was supplied from a burner as detailed in Figure No. 2 of TSO-C79.

The detector was immersed in the flame for a period of 5 minutes.

The system indicated a "Fire" when exposed to the flame and continued to indicate for the entire 5 minutes exposure.

After the 5 minute exposure the flame was extinguished and the system indicated "Fire Out".

The nature of the test did not permit system response times to be recorded.

System B, comprising C.W.U. Type 53813-202, Serial No. 100; C.C.U. Type 53813-204, Serial No. 100; Detector Type 53521-012, Serial No. XP3; Detector Type 53521-012, without serial number and fitted with fly leads, was subjected to the "Exposure to Flame" test as previously described.

The system indicated a "Fire" when exposed to the flame and continued to indicate for the entire 5 minute exposure.

After the 5 minute exposure the flame was extinguished and the system indicated "Fire Out".

It should be noted that during these tests a 270 kilohm resistor was incorporated into the emitter lines of the detectors which were immersed in the flame.

REFERENCES

- 2-1 Graviner Ltd. Drawing; UV Detector Dual Head; No. 53522-011-I.D., Rev. H.
- Graviner Ltd. Drawing; UV Detector I.D. (Single Head); No. 53521-012-ID, Rev. H.
- 2-3 Graviner Ltd. Drawing; Control Unit for Ultra-Violet Advanced Fire Detection System, System A; No. 53813-203GA, Rev. E.
- 2-4 Graviner Ltd. Drawing: Control Unit for Ultra Violet
 Advanced Fire Detection System, System B; No. 53813-204GA,
 Rev. E.
- 2-5 Graviner Ltd. Drawing; Circuit Diagram for Ultra Violet Advanced Fire Detection System A; No. 53813-203-CD, Rev. A.
- 2-6 Graviner Ltd. Drawing; Circuit Diagram for Ultra Violet Advanced Fire Detection System B; No. 53813-204-CD, Rev. A.
- 2-7 Graviner Ltd. Drawing; Drive/Supply Card; No. 43761-143-C.D., Rev. G.
- 2-8 Graviner Ltd. Drawing; Microprocessor Card; No. 43761-141-CD, Rev. B.
- 2-9 Graviner Ltd. Drawing; Logic Card Master for F-111 Application Only; No. 43761-142-C.D., Rev. F.
- 2-10 Graviner Ltd. Drawing; Logic Card Slave for F-111 Application Only; No. 43761-148-CD, Rev. D.
- 2-11 Graviner Ltd. Drawing; Common Output Logic Card; No. 43761-144-C.D., Rev. H.
- 2-12 Graviner Ltd. Drawing; Common Output Logic Card, System B; No. 43761-146-CD, Rev. F.
- 2-13 Graviner Ltd. Drawing; Battery Supply Card; No. 43761-140-C.D., Rev. B.

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- 2-14 Graviner Ltd. Drawing; Filter Board System A; No. 43765-028-CD, Rev. C.
- 2-15 Graviner Ltd. Drawing; Filter Board System B; No. 43765-029-CD, Rev. C.
- 2-16 Graviner Ltd. Drawing; Circuit Diagram of Crew Warning Unit; No. 53813-202-CD, Rev. D.
- 2-17 Graviner Ltd. Drawing; Advanced Fire Detection System Wiring; No. Z22004, REv. D.
- 3-1 Graviner Ltd. Drawing; Flow Diagram for Ultra Violet Advanced Fire Detection System; No. 53813-203/204-F.D., Rev. B.

APPENDIX A-1

PROCESSING OF ADJACENCY AND ABSENT HEADS INFORMATION

4.41

GRAVINER REPORT

TITLE

PROCESSING OF ADJACENCY AND ABSENT HEADS
INFORMATION FOR THE ADVANCED AIRCRAFT
FIRE DETECTION SYSTEM

AUTHOR/S

N.J.B. Young

NUMBER & DATE

R.242.

29th . January 1979

Checked by

N.J.B

Approved by

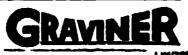
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ISSUE 2

PROCESSING OF ADJACENCY AND ABSENT HEADS INFORMATION FOR THE ADVANCED AIRCRAFT FIRE DETECTION SYSTEM

SUMMARY

The microprocessor systems fire and fault routines must allow for adjacency and for the possibility of installations with less than 8 pairs of heads. Earlier proposals for the scope of the system were not regarded as satisfactory by General Dynamics.

This report investigates the adjacency concept and describes a particular package which allows for 4 levels of adjacency and for up to 7 heads being absent. The suggested package has been designed to meet the current and anticipated future requirements of General Dynamics and to supersede the proposals of the interim report (D.840, 26th June 1978).



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- 1. Adjacency concept.
- 2. Design philosophy.
- 3. Head information.
- 4. Adjacency information.
- 5. First level adjacency.
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- 7. Third level adjacency.
- 8.
- Fourth level adjacency.
- 9. Adjacency tables.
- 10. Fire/Fault conditions
- 11. Adjacency set fire declaration
- 12. Schematic

Alternative definition of "seeing" a fire. Appendix 1.



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1. ADJACENCY CONCEPT

The system contains two microprocessors, A and B, each associated with one side of each pair of (up to) 8 U.V. heads (numbered 1, 2,). If there is no adjacency, any head may "see" a fire (a definition of "see" in this sense will be given later) and a fire condition for pair 1 is:-

Al sees a fire and Bl sees a fire

or, briefly,

Al and Bl

This fire condition is reset when both A1 and B1 cease to declare a fire

These rules are modified by adjacency. Let us declare the pairs 1 and 2 to be adjacent. Then the fire condition for this adjacency set becomes:-

((A1,A2), taken together see a fire) and ((B1, B2), taken together see a fire).

and the reset condition is that all four heads cease to declare a fire.

Having given an explanation of adjacency we now state some axioms.

- a) Adjacency is the same for the A and B sides of the system.

 If pairs 1, 2 and 6 (say) form an adjacency set we write (126)
- b) Adjacency is commutative.

 $(12) \Leftrightarrow (21)$

c) Adjacency of adjacency sets is equivalent to adjacency of their members.

(12 34)
★ (12 34)

Thus adjacency is associative





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We equate the adjacency set consisting of one head pair to that pair:

d) Adjacency is not transitive, in the sense that

12 and 23 \$ 123

We can therefore write the left hand side as (23), and (23) \Rightarrow (23)

It is desirable not to have transitivity as this enables greater design flexibility.

N.B. 123 should be read as "1, 2 and 3 form an adjacency set", not "1, 2 and 3 are adjacent". Therefore

as 1 and 2 do not form an adjacency set without 3, although 1 and 2 are adjacent. In this way we distinguish the descriptive property of "being adjacent" from the definitive logical property of forming an adjacency set.



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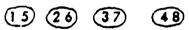
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2. DESIGN PHILOSOPHY

All the information determining the adjacencies and the number of heads for a particular aircraft system has to be hard-wired as 6 bits of a byte (whose other 3 bits are used for bit-serial data transfer and master/slave processor initialization). We then have a twin requirement that the method for encoding this information enables the widest possible range of configurations with the least amount of processing.

The design philosophy followed is to:-

- a) Cope with absent heads by making them adjacent to existent heads in an aircraft configuration, and using all 6 bits to contain adjacency information.
- b) Reconfigure these 6 bits into a small number of adjacency bytes which are combined with head information using logic and shift operations (avoiding branches and table look-up when possible) to give fire, reset and fault conditions.
- c) Remember that when the system is used to protect a single area it is preferable on reliability grounds never to have an adjacency set consisting of a single head pair. We could then insist a priori that every adjacency set consists of at least 2 pairs, in fact



(which will be termed "option PAIR") and that if one pair (say 4) is to be lone this can be achieved by omitting its adjacency partner (so 8 would not exist)

On the other hand we may require the system to protect two similar areas in which case we could insist that the adjacencies for 1, 2, 3 and 4 are repeated for 5, 6, 7 and 8, but that none of the first four is adjacent to any of the second four. (This will be termed "Option SPLIT")

Of course, although these options were originally designed for single area and two similar area systems respectively, they are of considerable use outride these applications. For the range of adjacencies possible see the sections below.

One of the 6 available bits will be used to choose between options PAIR and SPLIT. -10°

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N.B. i) Of course, fully to use the flexibility and power of this adjacency philosophy it is necessary to adopt intelligent numbering methods. Thus

may not be possible, but re-numbering 8 as 5 we can achieve (1.5)

ii) There is still the possibility of hard-wiring a single physical head pair into more than one location (to create a "ghost").

Thus:

can be achieved by wiring 5 into both 5 and 4, and using

Hardware requirements prevent a head being wired to more than two lines.

iii) As will be seen, the above philosophy enables relatively straightforward decoding/processing and considerable flexibility. We should note that the adjacency coding itself has a degree of redundancy (for example 4 independent pairs of head pairs may be configured as either of

Option PAIR = (15) (26) (37) (48)
Option SPLIT = (12) (34) (36) (78)

that its versatility increases dramatically when one or more heads are absent (as the numbering of the missing heads provides extra degrees of freedom) and that the choice of an appropriate numbering and configuration for a particular aircraft is a skilled operation.



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3. HEAD INFORMATION

(For easy reference this and later sections are summarised schematically at the end of this report).

Each U.V. tube is capable when energised of responding to incoming radiation by firing. A head firing causes the head to be de-energised for a (nominal) 2 ms recovery period and also makes available to the data bus a stretched pulse of (about) 1 ms. While in its gathering phase the microprocessor inspects the data bus 200 times at intervals of 832 μ s. Each stretched pulse will therefore be seen either once or twice. A second inspection of the same pulse is ignored; three successive sightings (1's on the data bus) must correspond to two pulses.

Therefore the sequence:-

0, 1, 1, 0, 1, 1, 1, 0

is processed (by setting to 0 the second 1 of a sequential pair) to

0, 1, 0, 0, 1, 0, 1, 0

and so on.

The stretched pulses in one gathering phase may be counted. If a count of 4 or more pulses per gathering phase is achieved by any head in an adjacency set, and this requirement is satisfied for three successive gathering phases, this adjacency set is said to see a fire. (For a fire condition to be issued it is necessary that at least one adjacency set see a fire un each of the A and B sides according to all processors working). An alternative definition of "seeing a fire" is given in an appendix. If a count of less than 2 pulses in a single gathering phase is achieved a head is said to clear. (For a reset to be issued it is necessary that all heads on both of the A and B sides in all previously fire-condition adjacency sets clear).

We wish to process the information for the eight heads (1 to 8) in parallel, and associate these heads with the eight bits (7 to 0) of a byte, thus:-

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HEADS	1	2	3	4	5	6	7	8	
BITS 7		· · - · · ·		·	· · · · · · · · · · · · · · · · · · ·	·	,		_ 0
		1		ł	Ì	}		1	

The 832 µs inspection byte is processed as follows:-

Inspection and (not, last true inspection) \rightarrow true inspection (alternative equivalent Boolean expressions exist).

Pulse counting is conducted using "Ones", "Twos" and "Fours" registers, (which must of course be zeroed at the start of each processing phase) and performing arithmetic in parallel thus:-

True Inspection and Ones

True Inspection Xor Ones

Carry-twos and Twos

Carry-twos Xor Twos

Carry-fours or Fours

Fours

Thus at the end of a gathering period, the Fours register has a 1 in each position where a head has fired at least four times. We now enter a processing period.

This side also has an F register, which as we shall see has a 1 in each position corresponding to a head in an adjacency set, which set is thought by its processor to see a fire. We generate a new register, the W register:

Four or (Twos and F) W

This register is to be made available to the other processor, via a DMA operation, in this form. Likewise a similar register, W^{I} , from the other processor has been received from the other side.



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3 (contd)

Another register, the H register, contains a 1 in each position corresponding to a head which passed the last test and is therefore assumed to be working. We make this available to the other side and have received their, H', register.

We now apply adjacency rules to these registers.



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4. ADJACENCY INFORMATION

I propose the following configuration of the byte containing the adjacency information ("configuration" byte).

Bit 0 = for bit-serial data transfer, not hard-wired.

1 = master/slave initialization bit.

2 = fourth level adjacency bit.

3 = third level adjacency bit

4,5,6 = second level adjacency bits

7 = first level (OPTION PAIR = 1, SPLIT= 0)

 Data Bus Bit
 7
 6
 5
 4
 3
 2
 1
 0

 Configuration byts
 1
 2 nd
 3
 4
 X
 X

At each level of adjacency we consolidate relevant data in the W, W', H and H' registers and fill the cleared spaces with 0's (W, W') or 1's (H, H'). The processing is the same for the W and W' registers, and for the H and H' registers.

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FIRST LEVEL ADJACENCY

If OPTION PAIR (bit 7 of configuration byte = 1)

(W or
$$\frac{4 \text{ spaces}}{W}$$
) and $11110000_2 \rightarrow W$

(H or
$$\stackrel{4 \text{ spaces}}{\leftarrow}$$
) or 000011112 \longrightarrow H

where the superscript arrow indicates a shift in the direction shown (not ring shift).

We can now treat the two options together, with the adjacencies for 1, 2, 3 and 4 repeated for 5, 6, 7 and 8.



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6. SECOND LEVEL ADJACENCY

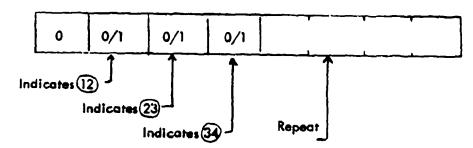
Reconfigure second level adjacency information :

Configuration and 01110000 -> Adj 2

Adj 2 or 4 spaces Adj 2

The upper and lower half-bytes of Adj 2 are identical and we describe only the processing associated with the former.

A one in a position of Adj 2 states that the corresponding head is adjacent to the head corresponding to the position on the left, this



The processing is:

W or (W and Adj2) and not $(Adj 2 \text{ and } (\text{not } \overrightarrow{Adj} 2)) \rightarrow W$ H or (H and Adj 2) or $(Adj 2 \text{ and } (\text{not } \overrightarrow{Adj} 2)) \rightarrow H$

H now has all ones except in the first position of an adjacency set (as so far specified) none of whose heads (on its side) are working. W now has ones in the first position of an adjacency set any of whose heads (on its side) have fired sufficiently often in the last gathering phase, and in no other position.



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7. THIRD LEVEL ADJACENCY

Third level adjacency may be used to declare the adjacency of lower level adjacency sets.

Take:

Adj 3 = 10001000 if third level adjacency bit = 1

Adj3 = 00000000"""""""""=0,

(i.e. no third level adjacency).

The processing is:

W or (W and Adj 3) and not Adj 3 -> W

H or (H and Adj 3) or Adj 3 -> H

Thus if we have the second level adjacencies

123

then third level adjacency can give

(123)

the relevant data being held in the head 2 (bit 6) position.

Note that third level adjacency should not be used unless the indicated second level adjacencies are declared. Failure to observe this may lead to a logical inconsistency and is forbidden.



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8. FOURTH LEVEL ADJACENCY

Fourth level adjacency may be used to declare the adjacency of lower level adjacency sets.

Take:

Adj 4 = 00100010

if fourth level adjacency bit = 1

Adj 4 = 00000000

" = 0

The processing is:-

W or (W and Adj 4) and not Adj 4 -> W

H or (H and Adj 4) or Adj 4 ---> H

Declaration of fourth level adjacency converts

1294

to

1 2 3 4

Fourth level adjacency should not be used unless the indicated lower-order adjacencies are declared. Failure to observe this may lead to a logical inconsistency and is forbidden.



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9. ADJACENCY TABLES

We list the permitted configuration bytes and generated adjacency sets.

•	aaja	cency	1013	•		
Split	lst	onfig 2nd			rte	Adjacency sets
	0	000	0	0	ХX	1 2 3 4 5 6 7 8
	0	001	0	0	XX	1 2 3 4 5 6 7 8
	0	010	0	0	xx	1 2 3 4 5 6 7 8
	0	011	0	0	XX	1 2 3 4 5 6 7 8
	٥	100	0	0	xx	1 2 3 4 5 6 7 8
	0	101	0	0	xx	12345678
	0	110	0	0	XX	12345678
	0	111	0	0	XX	12345608
	0	110	1	0	XX .	12345678
	0	111	1	0	xx	1 2 3 4 5 6 7 8
	0	111	1	1	XX	1 2 3 4 5 6 7 8
	Configuration byte		yte	Adjacency sets		
Pair	lst			4th	1434	
	1	000	0	0	XX	
!	1	001	0	0	XX	1 5 2 6 3 7 4 8
	1	010	0	0	XX	(13) (2 6 3 7) (4 8)
	1	011	0	0	XX	1 5 2 6 3 7 4 8
	1	100	0	0	XX	1 5 2 6 3 7 4 8
	1	101	0	0	xx	1 5 2 6 3 7 4 8
	1	110	0	0	XX	1 5 2 6 3 7 4 8
	1	111	0	0	xx	1 5 2 6 3 7 4 8
	1	110	1	0	XX	1 5 2 6 3 7 4 8
	1	111	1	0	XX	1 5 2 6 3 7 4 8
	1	111	1	1	xx	1 5 2 6 3 7 4 8



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) !

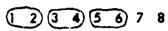
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9 (contd)

Note that none of the above adjacencies is equivalent to

1 2 3 4 5 6 7 8

01



which were mentioned in the interim report (D.840, 26th. June 1978)

Also note that we have used six configuration bits but only achieved 22 configurations, some of which are equivalent.

It is clear from the table that this adjacency system enables us fully to satisfy the current requirements of General Dynamics while providing a wide class of alternative adjacency arrangements should their requirements change.

The adjacency system has the further advantages of logical straighforwardness and of repetitive structure designed to enable efficient and economical programming.

The effect of the adjacency processing on W and H bytes is shown in a table in an appendix to this report.



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10. FIRE/FAULT CONDITIONS

The H, H', W and W' bytes have now been fully processed according to the adjacency rules. The W register has 1's in positions where heads of the relevant adjacency sets have fired the relevant number of times (and in no other positions). The H register is all 1's except in certain positions where all heads in the relevant adjacency set (on this side) are not working.

Therefore: -

 $H \text{ or } H' = 111111111 = FF_{10}$

unless all heads on both sides in at least one adjacency set are not working, in which case we issue a fault condition.

Under the current hardware arrangements a fault conditions overrides a fire condition, and latches. This arrangement may not be optional for future systems/installations, and there are advantages in writing the software in such a way as to enable alternatives to be implemented in hardware. The fault processing is:-

- i) If all the heads in an adjacency set on both sides of the system are not working a fault is issued and this set takes no further part in deciding whether there is a fire. (It is assumed that heads fail passive).
- ii) If all the heads in an adjacency set on one side of the system are not working (or are unavailable because that side is switched off or not present) then only the remaining side is considered.

Thus the complete failure of an adjacency set issues a fault but does not inhibit the processor from issuing a fire condition from other adjacency sets, though current hardware arrangements prevent the fire condition being sent to the CWU.

We combine the W and H registers by:-

W or (not H) -> W

W' or ((not H') and H) \rightarrow W'

noting that " is is the first till at the processing for the two sides has differed.



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10 (contd.)

We also have available the W registers for the previous three periods (now named the X, Y and Z registers) and also the similar X' and Y' (though not the Z') registers. The fire condition is to be issued by our microprocessor when it decides an adjacency set has seen a fire, on both sides, over the last three periods. As the data gathering periods for the two sides are interleaved there are of course two ways of choosing the three periods concerned, depending on which sides gathering phase starts the sequence.

We generate an F (for fire) register.

(W or Z) and X and Y \longrightarrow F

If (F and W' and X' and Y') $\neq 0$

we issue a fire condition for confirmation by the other processor, if working. Note that if this condition does no hold and a fire condition was already signalled, we do not rescind it; the reset process is defined below.

To derive the reset condition we use another register, the FL register, defined during the previous processing phase:

(F) and (W or W' or X or X') \longrightarrow FL

if the new FL = 0 we issue a reset.

The inclusion of X or X' terms allows the fire condition to be maintained if one gate period is not filled, however 2 consecutive empty gates will result in a reset condition.

Note that we have assumed both processors to be working in the above. If one is switched off or absent, the reset condition is altered in an obvious way.



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11. ADJACENCY SET FIRE DECLARATION

FL contains a 1 for each adjacency set now declaring an unreset fire state according to this processor side. We now have to reverse the adjacency processing and generate an F register to participate in the count of 2 or 4 decisions described above.

Fourth level = FL or (FL and Adj 4) → F
Third level = F or (F and Adj 3) → F

Second level = F or $(\overrightarrow{F} \text{ and Adj 2}) \rightarrow F$

First level = If OPTION PAIR, F or 4 spaces

Finally F has a 1 for each head in an adjacency set seeing a fire. (As a result, if a head is in two adjacency sets, its firing count requirement of 2 or 4 will be determined by either of the adjacency sets seeing a fire. This crosstalk only occurs when at least one side sees a fire, and is marginally beneficial.)

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ENGLAND

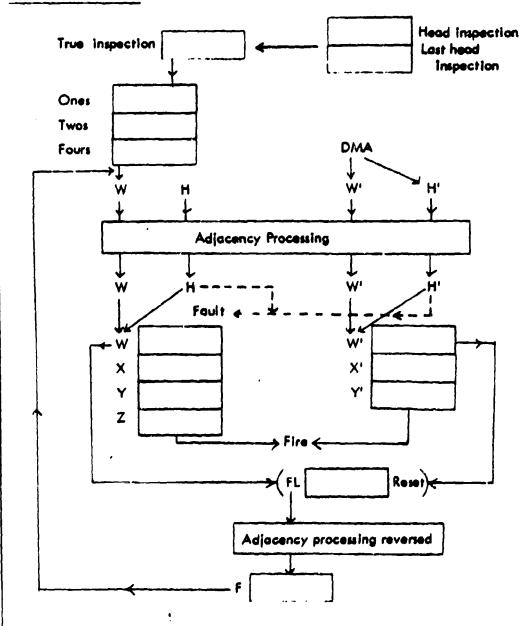
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12. SCHEMATIC



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APPENDIX 1

ALTERNATIVE DEFINITION OF "SEEING" A FIRE

The decision to perform the adjacency processing on the W and W' bytes implies and is implied by the definition of "seeing" a fire. We have defined this by adjacency set, requiring that for three successive gathering phases some head (not necessarily the same one) fires 4 or more times (on each of the A and B sides, according to all processors working.) An alternative and equally valid definition is to require the same head to fire 4 or more times for three successive gathering phases on side A, (and some head to do the same on side B, though by the adjacency these two heads need not belong to the same head pair.) Making this definition has implications for the probabilistic calculations of system reliabilities under different conditions, and for the methods of in-flight logging of fire and fault conditions. The change to the software is minimal however, it being necessary merely to perform the adjacency processing not on the W and W' bytes but on F and F', where these are derived from the unprocessed W, X, Y, Z, W', X', Y' bytes as

 $(W \text{ or } Z) \text{ and } X \text{ and } Y \longrightarrow F$ $W \text{ and } X \text{ and } Y \longrightarrow F$

APPENDIX A-2

SOFTWARE ASSEMBLY LISTING

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Data Sheets UU.5306
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               akeeti 13
                                                                                                                                                                     0131 07
0132 1740 ... X = 0
0133 DEC MPEG ... X = 0
0134 007 4
0125 TETPANT LDIROT PHI PA
0136 LDIRTO PLO PA
0137 LEP EVIT
   0202 F11
0004 721
                                                                                                                                                                                                                                                                                                                                       .. . . . DPADI
     ।।श्रद्ध ∄का
   0977 F201861
     HATA FRIDAKE
     626 D. Chakant
                                                                                                                                                                       UIST THE ENLY
UI
   0.200 $51
   HEDT FEADS
   0.000 0.200321
   nepe Consont
   HADA FAZSAAS
                                                                                                                                                                         #122 THHOPPE LDT OPADET PLO KPES
                                                                                                                                                                      1132 INDUPTION OF THE OFFICE O
   HEDE FORALOS
   OPER SAFAL
   HPEL ERLOFITSE
   HOER FORME 1791
     HOFO FAZAMAS
   APEC TERMS
                                                                                                                                                                          MINA LOVA PHI PA
     HOFE FRAGE
                                                                                                                                                                         HISS FUN PED BE
                                                                                                                                                                      HAFO FALDARI
   HOF . F441791
   02F6 34731
   1050 34731
   HIFA FREIGHT
   NAFR FANAFISAL
   0201 (004221
   0304 F325A21
                                                                                                                                                                     OF THE PROPERTY OF THE PROPERT
   HANT FORALMS
   0 20A 2A241
   DANG REPORTED
DATE BANGETON
   0914 F32664
   HALL TABLE
   maja smaat
                                                                                                                                                                          HE14 LDY PLO PA
                                                                                                                                                                     neta the plo Appa neta the plot of the control of t
  ONE ENDARI
 0915 #212731
0921 94731
0921 14771
 Hare Espanal
   naca manamphat
  ner Españas
                                                                                                                                                                       MESS LOP TINCHE WESS TIMELTS LOS OPADIS PLO MPEG HOP
  09:5 009341
 11年2月 - 南海沙馬南海6-41
 HATE PARALOS
                                                                                                                                                                         0224 ( DV ANTOLO
                                                                                                                                                                      1996 ESUSE1231
 0946 72P61
0948 60MM1
                                                                                                                                                                       HEEP LOVA PHI PS
                                                                                                                                                                       0220 LDK PLO PA
                                                                                                                                                                     1237 LDIDIO PLO MPES
1232 LDIDIO PLO MPES
1232 LDIDIA ITMD ... ITO EPROP CODE A3
1233 GHI PA ITMD ... OM LOC DOCID
1234 GLO PA ITMD ... TIME
1234 GLO PA ITMD ... TIME
1235 LDIDIA OP ITM MPEG
1235 LDIDIA OP O MPEG
1237 LDIDIA PLO MPEG
11948 F210921
11948 F22771
 0.450 36 771
  0952 34731
 0154 F32784F
 0257 F 104F 1531
 USED ENDOUGH
                                                                                                                                                                     USSE THE ELECHA
USSE THE ELECHA
USSE THINGS WED
 nase Couvable
 11261 1
 11341 1
                                                                                                                                                                       11,74 tr PNP
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173

anne

* Francisco

```
1 M
                         month $
                                   .. UPTE PATE ON LOCATION HORSE
.. THE PAPITY CATUL DATA IT TPANEMITTED FIRST
.. THEN THE DATA FROM LOCATION HORSE
00000-1
                         0.004
nona 1
                         4605
miner I
                                  .. IT COPYTED ON TO LOC UNCES AND DATA .. WILL BE TRANSMITTED. .. EACH BIT WILL BE TRANSMITTED THICE
10000 $
                         aan;
ம்ம்மும் இ
                         nna
កកម្មក រំ
                         111103
0000 1
                         0010
                         0011 .. FINALLY O IS PESET TO INDICATE 0012 .. THE END OF DWA ACTIVITY. 0013 EXIT#00600
                         0014 OPEROSBO
minn 1
                         ONIS LEND EXIT
HERD FRANCIS
OSP3 EAL
NSR4 FRESHALL
                         0017 LD1823 PLD P8
                         ONIS GHT PE AMINNI
11335° ARTII
                         6612 RE PEPEAT
114 bit 36.1
                         OUSU DOL ONE PR
HEPP FAFERAL
                         BOST ANTOFF PH! P6
                                                       .. PETET DHA POPT COUNTER
ned a not
                         OUS LIM FA
07/1 FAFF771
HT 4 TOFAHIS
HTC FITSE
                         10024 LEGA ANTON
                                                       .. PETET THE PIT ON O P ADDRETT
                                                       .. MEM LOCATION .. O P DATA TO POPT
                         0025 OP TP P2
1150 F 248
                         AUZA MEETI DUT 4
050 A 414
                         0027 001 1
                                                       .. TOGGLE DMA LINE
                        ONCY DOT 1
ONCY DEC PA
ONCY CLO PA
ONCY CENT FOR ONLY PA ANT HIN
050 B 364
.....
      4
of the semenal
or has a PALAS
OSD AF41
                         OURS PHT DUT
USDS FRIIPAL
                         4033 LDINII PHI PA
                                                      .. P6 = 110F
HADA FRIHAKT
                         0034 LDIBIO PLD P6
OSTO PS TOPOS
                        nus chinan PLD PA
OMBE TOKOL
OMBO MAL
                        ORSE LINE TRY
                                                       AL COPY MITO I LOC
USE1 CODECAL
                        0028 LAP EXIT
HEFT FRATRET
                        HARE DUTE EDINAL PHE PA
HEFT FEITHER
                        nuan i binin PLD PA
OSEA CACOOFOOS
                        HIGH PER LPP FEIT
HAFE MERGHIPAL
                        111142 PEPEATI GHT PA OPING PHT PA
056.2 (2004)
                        HILLS DEC PO LON PR
HTEU FRESE
076- -01
0867 -00-21
                        0014 TP
                        HHAP PR MEET
HTES 1
0006
```

: Fallagaille

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					, · · · · · · · · · · · · · · · · · · ·
FL	LOC	COSMAC	CODE	LNNO	SOURCE LINE
	0000			1	TEMPORARY SETTING OF SYMBOLIC NAMES
	0000			2	
	0000			3	•• OR ERROR CODE NOS
	9000			4	· · HEX VALUES APSOLUTE ADDRESSES
	0000			5	APOVE #ØC
	0000			6	• • UNPACK
	0000			7	NY VAL 2= #DF
	0000			8	NYVAL3=NYVAL2+4TO 4TH DMA LOCN
	0000			9	NY VAL 4= 47
	0000			10	. DECIMAL VALUE USED TO RESET
	0000			11	16 SEC (INTERRUPT) COUNTER
	0000			12	NYERRI=40 THIS SIDE
	0000			13	BEING INHIBITED
	0000			14	NYERR2=50 ADJACENCY BYTES
	0000			15	•• CHECK ERROR
	0000			16	NYCONF*RF
	9999			17	NYDEPK=RF
	0000			15	NY SCR=RA
	0000			19	NYSTA1=RB
	0000			20	NYCTR=RE
	0000			21	NYMAIN=R7 MAIN PROGRAM COUNTER
	9999			22	• RENEV
	9000			23	NYVAL5=#CANOT.H'.ANDNOT.H
	0000			24	
	9999			25	
	0000			26	NYVALS=#C7OLD H
	9999			27	
	0000			58	NYVALA=/D3 ··F
	0000			29	NYH=RF
	0000			30	NYSUB#R9 SUBROUTINES' COUNTER
	0000			31	NYADJ=RE
	0000			32	
	0800			33	· · · · · · · · · · · · · · · · · ·
	0000			34	
	0000			35	
	0000			36	
	9999			37	
	0000			35	
	0000			39	
	0000			40	
	0000			41	· · ADJSET
	0000			42	
	0000			43	
	0000			P 44	
	8888			45	
	0000			46	
	0000			47	
	0000			48	
	0000			49	··FLMGS INFU

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```
NYVALN=#2A .. #8C2A IS ROM CHECK TIMER,
9999
                          50
                                 .. # 0C29 IS 16 SEC(I/R) TIMER
0000
                          51
                                NYVALP=64 .. DECIMAL ROM CHECK RESET VAN
0000
                          52
                                NYVALQ=#42 .. ONES COUNT
0000
                          U3
0000
                          54
                                NYVALR=#40 .. FOURS COUNT
                                NYVALS=#26 .. MAIN TIMER (1 OF 2 BYTES)
                          55
0000
                                NYVALT=#20 ..W/H DATA (TO DMA)
0000
                          56
0000
                          57
                                NYVALU=#23 ..O/P BYTE
0000
                          58
                                NYVALW=#B5 .. LATCHED ERROR INFO
                                NYVALX=NYVALØ-1 ...NOT.H' PROCESSED
                          59
9000
                                NYVALY=#BC .. #OF FIRES LOCK
0000
                          60
                                NY VALZ=NY VALG-3
0000
                          61
                                HVALA=#C4..W COUNT HI
                          62
0000
                                HVALB=#54..COUNT STACK LEVEL 4
                          63
0000
0000
                          64
                                HVALD=#65..LEVEL 5 STORE
                                HVALE=#55 .. COUNT STACK LEVEL 5
0000
                          65
                                HVALF=#55
00005
                          66
                                HVALG=HVALD-16 .. END OF STORES
0000
                          67
0205
                          48
                                ORG #205
0205
                          69
                          78
0205
                          71
                                 .. UNPACK ROUTINE, PART OF FIRE ROUTINE
0205
0205 F825AB
                          72
                                NYVALK->NYSTA1.0
                                 .. POINTS TO INTERNAL FLAGS
0208
                          73
0208 0BFA10
                          74
                                ONYSTA1.AND.B'00010000'
                                  .. OTHER PROCESSOR STATUS
020B
                          75
                          76
                                IF 4>0 GO TO NYOFF!
020B 3A00
                                  .. SHORT BRANCH TO W', X', NOT.H'
                          77
020D
                                   .. SETTING ROUTINE
929D
                          78
                                 R0.0 .XOR. #FF ..ZERO FF CORRECT # 08
0200 BOFBFF
                          79
0210 3200
                          80
                                  IF=0 GO TO PS1
                                 .... IF NO DATA RECD., 2CASES
0212
                          81
                                 ... EF= 1, WE ARE INHIBITED
0212
                          SEP.
                                 ... EF=0, WE MUST INHBT OTHER PRCCSSR
0212
                          83
                                  IF NEFI GO TO NYOFFI
0212 3000
                          84
                                  ... HERE WE ARE INHBTD
                          95
0214
                                  ... FATAL FAULT FOR THIS SIDE
0214
                          86
                                  ... GRANCH TO LATCFL
0214
                          87
                                  ... WITH ERROR CODE IN D REG
                          88
0214
                                  NYERRIJLER LACHFL
0214 F828C00000
                          89
                                 PS1:NY VAL2->R0.0
0219 F8DFA0
                          90
                          91
                                   ... RESETS DMA PTR.
021C
                                  NY VAL 2- >NY DEPK . 0
                          92
021C FBDFAF
                                  ... POINTS AT LO BIT OF DMA DATA
                          93
921F
021F FF
                          94
                                  SEX NYDEPK
                          95
                                  91.X0R.0.AND.#84
0220 72F3FA04
                          96
                                  ... RESULT >0 IF 2 PORTS
0224
                                 .... CHECK BIT OK & DMA CRECT
0224
                          97
                                  IF>000 TO PS2
0224 3A00
                          98
9224 F829C00000
                          99
                                 #291LBR LACHFL
```

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	2005	AB		OCO-OCO NYDERY
	022E		100	PS2:DEC NYDEPK
		7276330072763300		0!/2'JBDF NYOFFIJ0!/2'JBDF NYOFFI
P. P.	-	72763B0072763B00	-	0!/2'JBNF NYOFFI;0!/2'JBNF NYOFFI
	023C		103	CHECKS FOR 0011 ON LOW
	023C	F60545	104	···4 DMA REGS(LO BITS)
		F8DFAF	105	NYVAL2->NYDEPK.0
		F8B9AA	106	NYVALI->NYSCR-0
		72FAFA5A	167	
		FOFAFA	108	O-AND-B'11111010' CLR OFF X BIT DATA
		EAF3	109	· · · · · · · · · · · · · · · · · · ·
_	02 4B		110	RESULT Ø IF L=R CONFIG
F		3200	111	
F		F830C00000	112	
		ØAFAF8FB88		PS3: 0NYSCR-AND-#F8-XOR-B '10001000'
	0257			CHECK FUR 4TH ORDER ADJ CASE
_	0257		115	· · · ZERO IF SAME
F		3A00 F8FC5A	116	IF>0 GO TO PS4 B'11111100'->•NYSCR
		F8D7AF	118	
		ØAFAFC5F	119	
	0263	NOT OF USE	120	···CONFIG TO LOCK
		FBDFAF	121	
	9266	FOUFMF	122	
	8546 8564		123	
	9244		123	
		F808AF	124	#08->NYCTR.0
	-	1F4F76	126	NYDKL1:INC NYDEPKJONYDEPK!/2°
	054C	ir mar fo	120	••LOADS BIT INTO DF
		F0765A2E	128	0/2'->ONYSCRIDEC NYCTR
	9279		129	• TRANSFERS BIT J'TO SCRATCH BYTE
	0270		130	NYCTR-0
		3A69	1 1	
	9273	Critis.	132	NB**UNPACKED STATUS LEFT
	0273		133	IN SCRATCH LOCK
	0273		134	**
	0273		135	NOW UNPACK H'/W' DATA IN SAME WAY
	0273	2A	136	DEC NYSCR . POINTS TO 2ND SCRATCH LOCK
	-	F808AE	137	#06->NYCTR-0
		1F4F76	138	NYDKL2:INC NYDEPKJONYDEPK!/2'
		F0765A2E	139	0/2'->ONYSCRIDEC NYCTR
	027E		140	NYCTR-0
		3A77	141	IF >0 GO TO NYDKL2
	0281		142	B. NYDEPK.O HAS MAX VALUE OF OFF
	0281		143	
	0281		144	
	0281		145	. THIS COMPLETES UNPACK ROUTINE
	0281		146	WILL CONTINUE IN FIRE ROUTINE
	0281		147	NR STATUS, W'/H' INFO LEFT
	0281		1 46	IN SCRATCH
	0281		149	
	•			

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```
150
0281
9281
                        151
                               ***********************
0281
                        152
0281
                        153
                                .. RENEW ROUTINE, PART OF FIRE ROUTINE
0281
                        154
                                 .. FOLLOWS UNPACK ROUTINE
                                 .. AUTHOR THIS SECTION .. NIGEL YOUNG
0231
                        155
0281 F82AAB
                        156
                               NY VALN->NYSTA1.0
0284
                        157
                                .. POINTS AT ROM CHECK TIMER
0284 1A
                        158
                               INC NYSCR .. TO POINT AT DMA'D OVER
0285
                        159
                                 .. STATUS BYTE
0285 0AFA08
                               ONYSCR-AND-B'00001000'
                        160
0288
                        161
                                ••1 IF ROM CHECK COMPLETED
0288 CEF8 40
                        162
                               LSZ JNYVALP
0288
                        163
                                 .. VALUE MUST NOT BE 0
0288 CESBSB
                        164
                               LSZJ->ONYSTA1J->ONYSTA1
028E
                        165
                                .. 2ND INSTRUCTION IS DUMMY FILLER
028E 0AFA04
                               9NY SCR . AND . B '00000100'
                        166
0291
                        167
                                ••0 FOR W', 1 FOR H'
0291 2A
                               DEC NYSCR .. TO POINT AT W'/H' BYTE
                        168
9292 3200
                        169
                                IF =0 GO TO NYOFF4
0294
                        170
0294
                        171
                                ...
0294
                        172
                                . . .
                                ..H' PROCESSING
0294
                        173
0294 2B
                        174
                               DEC NYSTAI
                                .. POINTS AT 16 SEC (INTERRUPT) TIMER
0295
                        175
0295 F82F5B
                               NYVAL 4-> ONYSTA! .. RESETS
                        176
                        177
0298 F8D6AF
                               NYVALX->NYH.0 ..POINTS
029B
                        178
                                ..AT .NOT.H' LOCATION
0298 EA
                        1 79
                               SEX NYSCR
                               A.0(ADJPR)->NYSUB.0
U29C F800A9
                        180
029F F800B9
                               A.1(ADJPR)->NYSUB.1
                        181
02A2 D9
                        182
                                SEP NYSUB .. CALLS ADJPR, RESULT LEFT IN
                                .. D REGR. NYADJ POINTS TO .NOT.DONTWOR
02A3
                        183
02A3 EE
                        184
                                SEX NYADJ
02A4 FRFFF2EF73
                                .XOR.#FF.AND.0->0-'NYH
                        185
02A9
                        186
                                 ..NYH NOW X REGR
                                 ..POINTS AT .NOT.H
02A9
                        187
0249 F800A9
                        188
                                 .O(HEADS) -> NYSUB.O
02AC F80089
                                  ((HEADS) -> NYSUB - 1
                        189
02AF 19
                        100
                                   NYSUB .. CALLS SUBROUTINE HEADS
0280
                        191
                                   HEAD FAULT ISSUING SUBROUTINE
9286 C00000
                        192
                                LBR NYOFFS
02B3
                        193
02B3
                        194
                                ...
02B3
                        195
                                ...
0283
                        196 NYOFF4: .. W' STORAGE
02R3 F8CDAF
                        197
                               NY VAL 6->NYH.0
0284 FF
                        198
                                SEX NYH
0287 72732F
                                01->0-1DEC NYH ..X'->Y'
                        199
```

Isaue: A

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* *

```
02BA 7273
                         200
                                0!->0-
                                                   ..W'->X'
                        201
                                ONY SCR->ONYH
02PC 0ASF
                                                  .. STORE W'
02BF C00000
                         202
                                LBR NYOFFS
                         203
02C1
02C1
                         204
                         205
                                . . .
02C1
02C1
                         206
                              NYOFF1:
9201
                         207
                                .. DEFAULT PROCESSING SETS W',X',Y'=#00,
                                  ...NOT.H'##FF, RAISES INHIPIT LINE, SO
02C1
                         208
                                 .. NO MORE DMA DATA SENT
02C1
                         209
92C1
                                .. SET OTHER PROCESSOR TO DEAD
                         210
                                 .. ON INTERNAL FLAGS. RAISE
Ø2C1
                         211
02C1
                                  .. INHIBIT BIT ON TRU AND O/P
                         212
02C1
                                  . . RAM LOCATION
                         213
02C1 F825AR
                                NYVALK->NYSTAI.0 .. INTERNAL FLAGS
                         214
                                PNYSTA1.OR.B'00010000'-> PNYSTA1
02C4 0BF9105B
                         215
02C8 2B
                         216
                                DEC NYSTAI .. TRU STATUS
02C9 0BF9085B
                         217
                                enystal.or.B'00001000'->enystal
                                DEC NYSTAL ..O/P BYTE
Ø2CD 2B
                         218
02CF 0BF9085B
                         219
                                enystal.or.B'00001000'->enystal
                         220
                                 SEX NYMAIN
02D2 E7
02D3 FBDFA0
                         221
                                 NY VAL 2->R0.0
02D6 AF
                         222
                                 PLO NYH
02D7 6200C4C4
                         223
                                 OUT 2,#00;NOP;NOP
                                 OUT 2,#00;NOP;NOP
02DB 6200C4C4
                         224
Ø2EF
                         225
                                 ...O/P TO GET A/C CONFIG
                                  ... NOP S FOR DELAYS
02DF
                         226
92DF EF
                                 SEX NYH
                         227
02E0 72F3FA04
                                 # ! . XOR . # . AND . # 64
                         228
                         229
                                  .. RESULT NON ZERO IF
02F4
92F4
                         230
                                 .. PORT CHECK BITS OK
02E4 3A00
                                 IF>0 GO TO PS5
                         231
                                 #F9;LBR LACHFL
02E6 F8F9C00000
                         232
02EB 2F
                                PSS: DEC NYH
                         233
02EC F8B9AA
                                  NYVALI->NYSCR.0
                         234
02EF 72FAFASA
                                  01.AND.B'11111010'->0NYSCR
                         235
02F3 FØFAFA
                         236
                                  0.AND.8'11111010' ... CLEARS OFF
                                  ...XBIT, DATA
02F6
                         237
02F6 EAF3
                                  SEX NYSCRI-XOR-
                         238
                                  .. RESULT NON ZERO IF L=R CONFIG
02F8
                         239
02F8 3200 $
                         240
                                  IF=0 GO TO PS6
02FA F830C90000
                         241
                                 #30;LBR LACHFL
                               PS6: ONYSCR.AND.#F8.XOR.B'10001000'
02FF 0AFAF8FB88
                         242
0304
                         243
                                  .. CHECK FOR 4THORDER ADJ CASE
0304
                         244
                                  . . ZEROØIF SAME
0304 3A00
                         245
                                  IF>0 GO TO PS7
                                  B:11111100 '- > eNYSCR
0306 F8FC5A
                         246
0309 F8D7AF
                                 PS7:NYVAL0->NYH.0
                         247
                                  enyscr.and.#FC->enyH..CONF TO LOCH
030C OAFAFCSF
                         248
0310 F8CEAFEF
                         249
                                NY VAL 7->NYH. 0; SEX NYH
```

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```
0314 F800737373
                           250
                                  NYVALX->NYH.0 ...NOT.H' PROCESSED
  0319 F8D6AF
                           251
                                  #FF->0- .. NOW POINTS AT .NOT.H
  031C F8FF73
                           252
                           253
                                  A.0(HEADS) -> NYSUB.0
  031F F800A9
                                   A.1(HEADS) -> NYSUB.1
  0322 F800B9
                           254
                                   SEP NYSUB .. CALLS SUBROUTINE HEADS
  0325 D9
                           255
                                    .. HEAD FAULT ISSUING SUBROUTINE
                           256
  0326
                           257
  0326
                                ...
                           258
  0326
                                 .. COMPLETES H', W' PROCESSING/STORING
                           259
  0326
                           260
  0326
  0326
                           261
                                NYOFFS: ... PROCESSING OR W STORING
  0326
                           262
                                   NYVALK->NYSTA1.0 .. INTERNAL FLAGS
                           263
  0324 F825AB
                                   ONYSTA1.AND.B '000000100'->NYH.0
  0329 08FA04AF
                           264
                           265
                                    .. EXTRACT 0 FOR W, 1 FOR H
  032D
                           266
                                    .. TEMPORARILY PUSH INTO N/II
  032D
                                   enyStal.and.2'11111011'->enyStal
  032D ØEFAFESB
                           267
                                    . . RESET
                           268
  0331
                                 ..!!!!!MUST RECHECK RESET USING
                           269
  0331
                                 .. LACHFL ROUTINE
                           270
   0331
                                   NYVALR->NYSTA1.0 .. FOURS COUNT
   0331 F840AR
                           271
                                   NYH-0 ... W OR H ?
                           272
   0334 8F
                                   LBZ NYOFF7 .. LONG BRANCH IF 0
                           273
  0335 C20000
                           274
   0338
                                   ...
                           275
   0338
                                   ...
   0338
                           276
                                   .. H PROCESSING
                           277
   0338
                                   .. FLAG ALREADY RESET
                           278
   0338
                                   NYVAL8->NYH.0 .. POINTS TO OLD H
   0338 F8C7AF
                           279
   033B EF
                           280
                                   SEX NYH
                                   UNYSTAL.XOR.#FF ..NEW .NOT.H
   033C ØBFPFF
                           281
   033F F2
                                   .AND. ... NEW-NOT. H. AND. OLD H
                           282
                                   IF=0 GO TO NYOFF8
F 0340 3200
                           283
                                   enystal.and.e->e-
   0342 0BF273
                           284
                                   NYVALS->NYSCR.0 .. TO BYTE OF MAIN TIMER
                           285
   0345 F826AA
                                   ONYSCR!->0-JONYSCR->0-
   0348 4A730A73
                           286
                                    .. RENEWS H, TIME
                           287
   034C
                                                        .............
                           288
   034C
                                 NYOFF8: .. PUT INTO DMA LOCATION
   034C
                           289
                                   NYVALT->NYSCR.0 .. STORE W/H FOR DMA
   034C F820AA
                           290
                                   WNYSTAI-> ONYSCR .. FOURS COUNT
                           291
   034F 085A
                           292
                                   NYVAL9->NYH.0
   0351 F8D5AF
                                    .. TO HOLD PROCESSED . NOT.H
                           293
   0354
                                   NYVALI->NYSCR.8 .. SCRATCH LOCK
                           294
   0354 F8B9AA
                           295
                                   enystal->enyscr .. UNPROCESSED H
   0357 0P5A
                                   SEX NYSCR
   0359 EA
                           296
                                   A.0(ADJPR)->NYSUB.0
                            297
   035A F800A9
                                   A.1(ADJPR)->NYSUB.1
   0350 F800B9
                            298
                                   SEP NYSUB .. CALLS ADJPR, RESULT LEFT
                            299
   0360 D7
```

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	00/1		200	IN D REGR, NYADJ POINTS TO
	0361		300	NOT.DONTWORRY BYTE
	0361	65	301	SEX NYADJ
	0361	<u>- '</u>	302	.XOR.#FF.AND.0->ONYH
		FBFFF25F	303	SEX NYH POINTS AT .NOT.H
_	0366	- - -	304 305	A.O(HEADS)->NYSUB.O
F		F800A9 F800B9	306	A-1(HEADSI->NYSUB-1
•	036D		307	SEP NYSUB CALLS SUBROUTINE HEADS,
	036E	07	308	HEAD FAULT ISSUING SUBROUTINE
F		F800A9	309	A.O(ADJSET)->NYSUB.O
F	_	F800R9	310	A.1(ADJSET)->NYSUB.1
	0374		311	SEP NYSUB . CALLS ADJACENCY BYTES
	0375	07	312	**RESETTING PROGRAM; D REGR CONTAINS
	0375		313	VALUE, NYADJ POINTS AT OLD VALUE OF
	0375		314	. SUM CHECK BYTE
	0375		315	SEX NYADJ
	0376		316	•XOR•● ••SHOULD BE ZERO
F		3200	317	IF #0 GO TO NYOFF9
•	0379	3200	318	OTHERWISE FATAL ERROR FOR
	0379		319	THIS SIDE. BRANCH TO FAULT
	0379		320	LATCHING SECTION WITH ERROR
	0379		321	CODE NO IN D REGR
F		F832C00000	355	NYERRZILBR LACHFL
•	037E		323	
	Ø37E		324	
	037E		325	•••
	937E		326	W STORAGE
	937F		327	NYOFF7: NYSTAI POINTS AT FOURS COUNT
	037E	FBD3AF	328	NYVALA->NYH.0POINTS AT F
	0381	F820AA .	329	NYVALT->NYSCR.0STORE LOCN
	0384		330	FOR DMA ACROSS
	0384	EB60	331	SEX NYSTALLIRX POINTS AT TWOS
	0386	0ff2	332	enyh.and.#(Twos)
	0388	28	333	DEC NYSTAI
	Ø389	F15A	334	.OR.@(FOURS)->@NYSCR
	MARR		335	··STORES FOR DMA
	038B	2F2FEF	336	DEC NYHIDEC NYHISEX NYH POINTS AT Y
	938F	72732F	337	
•	0391	72732F	338	01->0-JDEC NYHX->Y
		7273	339	0!->0-
		ØASF	340	enyscr->enym
	n398			
	0398		342	•••
	0398		343	•••
	#398	_	344	NYOFF9: REJOIN
	9398	7 B	345	SEO SETTING O ALLOWS DMA OUT
	0399		346	TO OTHER SIDE
	0399		347	NB NYSCR NOT RESET HERE
	0399		3 48	
	0399		3 49	

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```
0399
                           350
                                   .. THIS COMPLETES RENEW ROUTINE, NOW
   0399
                           351
                                    .. ENTER FSET, FINAL PART OF FIRE ROUTS
   0399
                           352
   0399
                           353
   0399
                           354
   0399
                           355
   0399
                                   .. FSET ROUTINE, LAST PART OF FIRE ROUTE
                           356
                           357
                                    .. FOLLOWS RENEW ROUTINE
   0399
   0399
                           358
                                    .. AUTHOR THIS SECTION. . NIGEL YOUNG
   0399 F8C4AEEE
                           359
                                   NYVALB->NYADJ. ØJ SEX NYADJ
   039D
                           360
                                    .. POINTS TO LOCK OF LOGGED NONZERO W E
   039D F825AF
                           361
                                   NYVALK->NYW.0
   03A0 0FFA80
                           362
                                   enyw.and.B'10000000'
                                  LBNZ NYOFFA
N 03A3 CA0000
                           363
                           364
                                  ..... W.X,Y,Z,W',X',Y'L LOGGING
   03A6
   03A6 F8CFAF
                           365
                                     NYVALC->NYW.0
   03A9 0F
                           366
                                      ONYW
   03AA 3200
                           367
                                      IF=0 GO TO HB
   03AC F8C4AA
                           368
                                      HVALA->NYSCR.Ø
   Ø3AF EA
                           369
                                    SEX NYSCR
   0380 F0FBFFC20000
                           370
                                    .XOR. #FFILBZ HA
   03BA 2A
                           371
                                    DEC NYSCR
   0387 72AFF0BF
                           372
                                    0!->NYADJ.010->NYADJ.1 ..W COUNT->REG
   03BB F808AB
                           373
                                      #8->NYSTA1.0
   03BF 0F765F
                           374
                                    HST: ONYW/2'->ONYW ..LSB TO DF
                           375
                                      LSNF .. IF Ø DONT INC
   03C1 C7
   0302 1EØF
                                      INC NYADJIONYW.. COUNT 1 IF NOT 0
                           376
   03C4 2B
                           377
                                      DEC NYSTA1
   03C5 8B
                           378
                                      NYSTA1.0
   03C6 3ABE
                           379
                                      IF>0 GOOTO HST.. TOTAL OF 8 TIMES
                                      enyw/2 '-enyw.. RESTORE W
   03C8 0F765F
                           380
   03CB 9E5A
                           381
                                      NYADJ.1-> ONYSCR.. REPLACE W COUNT HI
   03CD 2A
                           382
                                     DEC NYSCR..LEFT AT FIRST W COUNT
                                      NYADJ.0-> ONYSCR. . REPLACE W COUNT LO
   Ø3CF 8E5A
                           383
   03D0 F80CBE
                                    HA: NY VAL->NY ADJ-1 ... RESET U/BYTE TO 6
                           384
   0303
                           385
                                  0303 F855AA
                           386
                                   HB:HVALF->NYSCR-0
   0306 EA
                           387
                                      SEX NYSCR
                                      #00->0-,0-,0-,0-,0-
   0307 F8007373737373
                           388
   03DF, F8FF73
                                      #FF-> - .. STACIHBSET
                           389
                                      A.Ø(ADUP)->NYSTA1.Ø
   03F1 F800AP
                           390
   03F4 F800PB
                           391
                                      A.I(ADUP)->NYSTAI.I.. SET TO ADUP SUE
   03E7 F8CCAE
                           392
                                      NYVALD->NYADJ.0..W'OLOCN.
                                      SEP NYSTAI . . GO TO ADUP SUB.
   03FA DR
                           393
   03EB IE
                           394
                                      INC NYADJ .. X'
                           395
                                      SEP NYSTAL . . GOSUB
   Ø3EC DB
   03ED 1F
                           396
                                      INC NYADJ .. Y'
   Ø3EE DB
                           397
                                      SEP NYSTAL
   03EF 1E1E
                           398
                                      INC NYADJ; INC NYADJ.... X
   MSF1 DB
                           399
                                      SEP NYSTAI
```

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<u>4</u> >

```
CF2 1E
                             400
                                       INC NYADJ.. Y
    03F3 DB
                             401
                                       SEP MYSTAL
    03F4 F8CFAF
                             402
                                       NYVALC->NYW.8..W LOCN.
    03F7 FBASFCOIAT
                             403
                                       HVALD+1->NYADJ.0 ..W.OR.Z (SCRATCH)
    03FC 0F
                             404
                                       BNYW
                                              . . W
    03FD IFIFIF
                            405
                                       INC NYWIING NYWIINC NYW ...Z
    0400 EF
                            406
                                       SEX NYW
    0401 F15E
                                       .OR.4->#NYADJ ...W.OR.Z
                            497
    0463 DE
                            408
                                       SEP NYSTAL
   0404 3000
                            409
                                       GO TO ADEND
    0406
                                   ..... SUBFOUTINE ADUP
                            410
    8406 D7
                            411
                                       SEP NYMAIN
   8487 F854AA
                            412
                                     ADUP: HVALE -> NYSCR. 0
   048A FA
                            413
                                       SEX NYSCR
   040B 0FF2
                            414
                                       enyadj.and.e ... NEW 5 COUNT
   040D 60
                            415
                                       IRX ... 5 LOCN.
   040F F1732A
                                       .OR. 0->0-JDEC NYSCR ... STORE & MOVED
                            416
   9411 BEF2
                                       enyadj.and.e ... NEW 4 COUNT
                            4170
   0413 60
                            4180
                                       IRX
   0414 F1732A
                            419
                                       .OR. 0->0-JDEC NYSCR
   0417 0EF2
                            428
                                       enyadj.and.e ... NEW 3 COUNT
   8419 68
                            421
                                       IRX
   041A F1732A
                            422
                                       .OR. -- > - : DEC NYSCR
   0410 0FF2
                            423
                                       enyadj.and.e ... NEW 2 COUNT
   041F 60
                            424
                                       IRX
   0420 F173
                            425
                                       .OR.0->0-
   0422 0EF173
                            426
                                       PNYADJ.OR. e->e-
   0425 60
                                      IRX
                            427
   0426 3006
                            428
                                       GO TO ADUP-1
   0428
                            429
                                  ..... END OF ADUP
   0428 F826AE
                            430
                                    ADEND: NYVALS->NYADJ.0 ... MAIN TIMER S
   0428 F80CBB
                            431
                                      NYVAL->NYSTA1.1 ... RESET U/BYTE TOO
   042F F855AA
                            432
                                      HVALE->NYSCR.0 ... 5 COUNT
   0431 F865AB
                            433
                                   FIVES: HVALD->NYSTA1.0
   0434 0A2A
                            434
                                   HC: ONY SCR! DECNY SCR
F 0436 3200
                            435
                                      IF=0 GO TO FOURS
   0438 EB73
                            436
                                      ->e- 'NYSTAI
   043A 4E738E739F
                           437
                                     ONYADJ!->0-10NYADJ->0-1DEC NYADJ
F 043E F0FBFF3200
                           438
                                     #.XOR.#FF; IF=0 GO TO HD
  0444 F0FC015B
                           439
                                    #+1-> ONYSTA1
  0448 8BFC03AB
                           440
                                    HD:NYSTAL . 0+3->NYSTAL . 0
  044C 8BFF04AB
                           441
                                   FOURS: NYSTA1 . 0 - 4 -> NYSTA1 . 0
  0450 8BFF55
                           442
                                     NYSTAL . 0 - HVALG
  0453 CE
                           443
                                     LSZ
  0454 3034
                           444
                                     GO TO HC
  0456
                           445
                                     ..... END OF LOGGING
  0456
                           446
                                   . . . .
  0456
                           447
                                   ...
  BASK FECCAP
                           448
                                NYOFFA: NYVALD->NYW.0
  0459
                           449
                                    .. POINTS TO W'
```

1.13

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	0459	e.	450	SEX NYW
		F8B9AA	451	NYVALI->NYSCR-0SCRATCH LOCK
		72F1	452	0!.OR.0W'.OR.X'
		6060	453	IRXJIRX
		F160	·	• OR • • (W) # I RX
	0463		· - ·	•0R••(X)
		606060		IRXJIRXJIRX
		F25A	457	•AND••(F)->•NYSCR
	8469	F & J ~	458	RESET CONDITION BYTE IN DUMMY LOCK
	0469		-59	
	0469		460	•••
	6469		461	NOW CALCULATE F
	0469	2F	462	DEC NYW POINTS AT Z
		FØ2F2F2F	463	O(Z);DEC NYWIDEC NYWIDEC NYW
		F160	· 	.OR. 0(W); IRX
		F260		•AND••(X);IRX
		F2EAF1		.AND. #(Y).OR. # 'NYSCR
		2A5A		DEC NYSCRJ->ONYSCR
F		F800A9	468	A.)(ADJPR)->NYSUB.0
F	047A	F800B9	469	A (ADJPR)->NYSUB.1
	947D	D9	470	SEP NYSUB CALLS ADJPR
	847F	•	471	RESULT LEFT AT SCRATCH LOCK
	047E		472	NYADJ POINTS TO .NOT.DONTWORRY
	847E	ØEF25A	473	enyadj.and.e(F)->enyscr
	0481		474	DONTWORRY PROCESSING
	9481	F8D5AF	475	NYVAL9->NYW-0
	0484		476	POINTS AT .NOT.H
	0484	0FF15A	477 .	ONYW.OR.O(F)->ONYSCR
	9487		478	F SAVED IN SCRATCH LOCK
	9487		479	•••
	0487		480	**
	0487		48 1	··NOW CALCULATE F'
	0487	IA	482	INC NYSCR TO POINT AT RESET BYTE
	0488	FBCCAF	483	NYVALD->NYW.0 POINTS TO W'
	048B	ë e	48 4	SEX NYW
	Ø48C	72F260		#!.AND.#JIRXW'.AND.X'
•	048F	F2EAF15A		.AND.O(Y').OR.O'NYSCR->ONYSCR
F		F800A9	48 7	A.0(ADJPR)->NYSUB.0
F		F800B9	488	A.1(ADJPR)->NYSUB.1
	0499	N9	-	SEP NYSUB CALLS ADJPR
	049A		490	RESULT LEFT AT SCRATCH LOCK
	049A		49 1	NYADJ POINTS TO .NOT.DONTWORRY
		ØEF25A	492	enyadj.and.e(f')->enyscr
		F8D4AF	493	NYVALF->NYW.0 POINTS TO
	04A0		49.4	(H.AND.(.NOT.H'))
		ØFF1	495	PNYW.OR. PC.
	04A2		496	DEC NYSCR POINTS AT F
		F25A	497	.AND.O(F'.AND.F)->ONYSCR
	04A5		498	NYSCR POINTS TO FIRE CONDITION BYTE
	04A5		499	

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	04A5		500	••• *
	04A5	1.6	501	INC NYSCR
			502	->enyscridec nyscr
•	_	SAZA	503	IF NO FIRE AUTOMATICALLY
	04A8 04A8		504	CONTAINS #00 FOR RESET
		F825AF	505	NY VALK->NYW.0
	04AB		506	•NYSCR
F	04AC	•	507	IF>0 GO TO POINT!
		OFFA7FSF	508	•NYW.AND.B'01111111'->•NYW
	04R2	OFFM /F DF	509	. RESET HEAD TEST FLAG
F	0482	2000	510	GOO TO POINT4
•		0FFA8 0	511	POINT1: 0NYW . AND . B . 100000000
_	(04B7		512	IF >0 GO TO POINTS . DON'T LOG
r		F8C2AF	513	NYVALG->NYW-0OLD F&F' LOCK
		F826AB	514	NYVALS->NYSTA1.0TIMER
	04RF		515	ONYW
-		3200	516	IF=0 GO TO LOG
F		_	517	NYVALZ->NYW.Ø2ND LOG LOCN
		FBBFAF	51 <i>7</i> 518	LOG: ONYSCR-O- 'NYW
		0AEF73	519	•NYSTA! -> •- J •NYSTA! -> •-
		48730873 F823AB	520	POINT2:NYVALU->NYSTAI-0O/P BYTE
		0BFA04	521	ONYSTA1.AND.B'00000100'
_	- • -	•	521 522	IF >0 GO TO POINJ3
F		JAUU	523	•• FIRE NOT ABOUT TO BE SET
	04D4	-c0c40	-	NYVALY->NYSTA1.0# OF FIRES LOCK
	-	F8BCAB	524 525	enystal-cff
_		0BFFFF		· · · · · · · · · · · · · · · · · · ·
•		3200	526	IF =0 GO TO POINT3REG. FULL ONYSTA1+#01->ONYSTA1INCREMENT
	_	ØBFCØ15B	527 528	POINT3: B '00000100'-> ONY SCR
	_	F8045A	529 ●	POINT 4: SEX NYSCR
	04E3		527 V 530	NYVALU->NYSTAI.0O/P BYTE
		F823AB	-	ONYSTAL AND B'11111011' OR O->ONYSTAL
		ØBFAFBF15B	531 530	SETS OR RESETS O/P FIRE CONDITION
	0 4F.C		532 533	SEX R7
	94EC		534	DI 5, #77
		7177	535	SEX NYSTALLOUT 4
		EB64	536	OUTPUTS
	0 4F 1	6 A		*** = *
	04F1	OBFAFBF15B	537 538	ONYSTA1.AND.B'11111011'.OR.C->ONYSTA1
			539	
	04F7	7077EA	540	RET. #77; SEX NYSCR
		10 / / F.M	541	SAVES FIRE IN TRUE LOCHSALSO
	0 4FB		542	••*
	04FB		543	**
	0 4FD		544	.NOW REVERSE ADJACENCY PROCESSING
	04F8		545	OF F; USE 3 REGR. SOFOR CONVENIENCE
	04FE		546	CAN USE JUIT 2
	04FP	1 Δ	547	INC NYSCR
	04FC	1 77	548	POINTS TO F.AND. F'OIN SCRATCH
		F8D3AF	549	NYVALA->NYW.0
	var C	roughr	347	IA C.

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	04FF	550	POINTS TO SAVE LOCH OF F
	04FF F8DBAE	551	NYVALJ->NYADJ-0
•	0502	552	POINTS TO ADJ1
	0502	553	REVERSE IST LEVEL ADJ PROCESSING
	0502 0AF6F6F6F6	554	ONYSCR/2/2/2
•	0507 EEF2EAF15A	555	-AND-0'NYADJ-OR-0'NYSCR->ONYSCR
	050C	5560	* REVERSE 4TH LEVEL ADJ PROCESSING
	050C 2E	5570	
	050D F6EEF2EAFISA	558	/2.AND.0'NYADJ.OR.0'NYSCR->ONYSCR
	0513	559	REVERSE 3RD LEVEL ADJ PROCESSING
	0513 2E	560	DEC NYADJ
	9514 FEEFF2EAF15A	561	#2.AND.0'NYADJ.OR.0'NYSCR->0NYSCR
	051A	562	REVERSE 2ND LEVEL ADJ PROCESSING
	051A 2E	563	DEC NYADJ
	051B F6FFF2EAF15F	564	/2.AND.0'NYADJ.OR.0'NYSCR->ONYW
	0521	565	SAVES F FOR NEXT ENTRY TO FIRE ROUTE
	0521	U66	NOW RESET FOURS, TWOS, ONES COUNT
	0521 FB 42AA	567	NYVALO->NYSCR.0 ONESOCOUNT POINTER
	0524 F800737373	568	100->0-,0-,0-
	0529	569	END OF PROGRAM SECTION FSET
	0529	570	WHICH COMPLETES FIRE ROUTINE
	0529	571	
	0529	572	
	0529	573	ENDS FIRE ROUTINE
	0529	574	****************************
	0529	575	NOW CHECK DMA RAM
	0529 EF	5760	SEX RF
	052A F8FFAF	577	LDI#FF;PLORF
	052D F8AA738F	578	POINT:LDI#AA; STXD; GLOORF
	0531 FFDE3A2D60	579	SMIPDEJBNZ POINTJIRXTO POINTAT DE
F		580	REPT:LDXA; SMI #AA; BNZ WRONG
,	0538 8F3A362F	581	GLOORFIBNZ REPTIDEC RF
	053E F855738F	582	AGIN:LDI#55; STXD; GLO RF
	0543 FFDE3A3F60	583	SMICDEJBNZ AGINJIRX
F	9548 72FF553A00	584	ROUND: LDXA; SMI#S5; BNZ WRONG
F		585€	GLOORFJBNZ ROUNDJBR RIGHT
5		586	WRONGILDI#24JLBR LACHFL
	0557 F80CBFB0F8E2AF		
	055E0F8007373	588	LDI 01STXD1STXD
	0562 F8FF7373	589	LDI#FF;STXD;STXD
	9566€	590	SET 1ST 4 DMA LOCKS
	05660		TO INDICATE FAILURE
	9566	592	*******************************
	0566 F8DFA0	5930	LDI#DF;PLO RO . RE-INITIALIZE DMA
	0569 F825AF0F	594	LD1#25/PLO RF/LDN RF
	056D FAFESF	595	ANI#FE;STR RF
	0570 D3	596	SEP RO
	● 0 800	597	ORG #800
	0800	598	
	0800	599	SUBROUTINE ADJSET, AUTHOR NIGEL YOUNG
		J	1.4.

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```
0800
                           600
                                  .. CALLED BY INITIALIZATION
 0800
                                  .. AND 15 SEC H SETTING ROUTINES
                           601
 0800
                           602
                                ADJSET:
 OPOO FEDTAFAE
                           603
                                  NY VAL 0->NYCONF.0.NYADJ.0
 0804
                           604
                                    .. CONFIG BYTE
 0804
                           605
                                   .. USE NYADJ TO POINT TO
 0P04
                           606
                                    .. ADJACENCY BYTES
 9894
                           607
                                   .. NB UPPER BYTEOOF REGRS
 0804
                           608
                                    .. MUST BE #0C
 6304 F8B9AA
                                  NYVALI-NYSCR-0 .. SCRATCH
                           609
                                     .. PUT LOCATION INTO WHAT WILL BE X RE
 0807
                           610
 0807 4EEA73
                           611
                                  enyabj!->e- 'nyscr
  BBBA
                           612
                                   .. INCREMENTS NYADJ
  080A
                           613
                                    .. DECREMENTS NYSOR (WH BECAME X REGR)
  ØBØA
                           614
                                    .. PUTS CONFIG INTO IST SCRATCH LOCATIO
  OPOA
                           615
                                     . .
 080A
                           616
                                     . .
 BOA
                                   .. NOW CREATE ADJ2
                           617
 ØBØA
                           61X
                                    .. CONFIG ALREADY IN D REGR
  BROA FA705A
                           619
                                   &.AND.8'01110000'-> ONYSCR
 080D F6F6F6F6F13E3A
                           620
                                   1/2/2/2/2.OR>0~>0NYADJ, 0NYSCR
 0B14
                           621
                                    .. ADJ2 STORED IN ITS AND DUMMYOLOCH
 0814 72F473
                           422
                                   #!+#->#- .. CONFIG+ADJ2 STORED
  0B17 4EFEFBFFF25A0
                                  enyadj: +2.xor.#ff.and.e->enyscr
                           623
  081D
                                     .. PART CALCULATION OF DONTWORRY BYTE
                           624
  ØBID 60
                           625
                                  IRX . . REINCREMENTS TO POINT ATOSUM TOTAL
  OBIE
                           626
  ØBIE
                           627
                                   .. NOW FIND ADJ3
  0B1E
                           628
                                   .. FINDING OF ADJ3, ADJ4, ADJ1 COULD BE
  OBIE
                           629
                                    .. WRITTEN AS COMMONOSUBROUTINE
  081E
                           630
                                    .. BUTONODADVANTAGE IN CODE LENGTH
  0B1E00FFA08
                           631
                                   #NYCONF.AND.B'00001000'->&M
                                                                     6821 CER
  0822 F888
                           633
                                  8'10001000'->4 .. ELSE SET TO VALUE
● 0B24 5E
                           634
                                   4-> NYADJ
  0825
                           635
                                    .. STORES ADJ3, EITHER @ ORDSET VALUE
  0B25 F473
                           636
                                   4+0->0- ..SUBTOTAL
                                   enyanji.or.e->enyscr
  0827 4FF15A
                           637
                                    .. PART CALCH OF DONTWORRY BYTE
  082A
                           638
                           639
                                   IRX .. INCREMENT X REGR
  082A 60
  082B
                           640
  OP2B
                           64100
                                   .. NOW FIND ADJ4 SIMILARLY
  OP28 OFFA04
                           642
                                  enyconf.and.8'00000100'->4
  OBSE CE
                           643
                                  LSZ
  ØB2F F822
                                  B'00100010'->&
                           644
  0831 5E
                           645
                                   L->enyabj
                                   1+0->0-
  0832 F473
                           646
  0P34 4EF15A60
                                  enyadji.or.e->enyscr: Irx
                           647
  ØBJ8
                           648
  0838
                           649
                                   .. NOW FIND ADJI SIMILARLY
```

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		·		
		OFFA80	650	ONYCONF.AND.B'10000000'->4
	Ø838	· -	651	LSZ
•	ØB3C		652	B'00601111'->&
	0B3E		653	&->ONYADJ
	083F	F 473	6540	
	0B41		655	PARTIAL SUM SAVED
	Ø841		656	••
	ØB41		657 €	NOW CALCULATE .NOT. DONTWORRY
		4EF1FRFFSE	658	enyadj!.or.e.xor.#FF->enyadj
	0B46		659	INC NYADJIIRX
	0P48	IF 4	660	8+0->8 PARITY SUM CHECK BYTE LEFT
	0B 49		661	IN D REGR. X REGR LEFT POINTING AT
	0B 49		662	• SUM SCRATCH LOCATION WHICH ONLY
	ØB 49		663	CONTAINS PARTIAL SUM WHICH SHOULD
	0849		664	. NOT BE USED
	0849		665	NYADJ LEFT POINTING AT PARITY SUM
_	ØB 49	5.5	666	BYTE, NYPARI, LOCATION
•	ØB 49		667	SEP NYMAIN RETURN
	084A	•	668	END OF SUBROUTINE ADJSET
	0B4A		669	
9 0	08 4A		670	***************************************
	084A		671	
	084A		672	•••
•	0B4A 0B4A		673 67 <i>4</i>	*SUBROUTINE HEADS.CALLED IN PROGRAM
•	00 4A		675	SECTION RENEW
	7 / P		676	ISSUES FAULT ON HEAD FAILURE THRUOUT
	02 4A		677	ANY ADJACENCY SET
	0P4A		678	.AUTHOR THIS SUBROUTINE . NIGEL YOUNG
	0E 4A	•	679	HEADS:
	0E 4A		686	X REGR IS NYH, POINTING AT .NOT.H
	OF 4A		681	.ENTER HERE
		F8B9AA	682	NYVAL1->NYSCR.0 SCRATCH
	CP4D		483	MUST ENSURE NOT OTHERWISE NEEDED
		72FEFFF2	68 4	01.XOR.#FF.AND.0
	0851	- · -	685	DEC NYHADEC NYH
	0253	-	686	->ONYHSTORES (.NOT.H').AND.H
	0P54		687	INC NYH
	0855	72F25A	688	@!.AND.@->@NYSCR(.NOT.H').AND.(.NOT#
	0858		689	IF NOT ZERO, FAULT
O F	0B58	3200	690	IF =0 GOOTO NYOFF6 RETURNS
•		FBCAAF	691	NYVAL5->NYH.0
	0B5D	0F	692	ONYHOLD VALUE OF (.NOT.H').AND.(.NO
F		3A00	693	IF >0 GO TO NYOFF6 DONT RENEW IF
	ØB 60		69 4	AL READY NON-ZERO
	0840	ØA73	695	ONYSCR->O-
•	88 48	E826AA	696	NYVALS->NYSCR.0TIMER
	0P45	4A73ØA73	697	Onyscr!->O-Jonyscr->O-
•	0 B69		698	LOGS FAULT
	0B69	F823AB	699	NYVALU->NYSTA1.0O/P STATUS

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```
700
                                enystal.or.B'00000010'->enystal
086C 08F9025B
                         701
                                INC NYSTAI
0B70 1B
                                enystal.or.B'00000010'->enystal
0871 08F9025B
                         702
                                 .. SAVES FAULT INTERNALLY & FOR O/P
                         703
0875
                         704
                                 ..??NEED TOOCHECK FAULT BUTTON
Ø875
                         705
                              NYOFF6: SEP NYMAIN .. RETURN
0875 D7
ØB76
                         786
                                 .. END OF SUPROUTINE HEADS
0876
                         707
0B76
                         708
                         709
BR76
0876
                         710
                         711
0876
                                 .. SUBROUTINE ADJPR, AUTHOR NIGEL YOUNG
0876
                         712
                                 .. CALLED FOR F,F',H,H' PROCESSING
                         713
0B76
                         714
                              ADJPR:
ØR 76
9876 FBD7AF
                         715
                                NYVALO->NYADJ.0 .. CONFIG
                                  .. SAVES FAILT IN TRUE LOCATION ALSO
ØB79
                         716
                                  .. USE NYADJ TO POINT TO ADJACENCY BYTE
                         717
0B79
                                  .. N.B. UPPER BYTE MUST BE #0C
                         718
ØR79
                         719
                                 INC NYADJ
0879 1E
087A 4EF2FEF17360
                         720
                                 enyadj!.and.e=2.0R.e->e-; IRX
                         721
                                  .. PERFORMS SECOND LEVEL PROCESSING
BRRB
0880 4EF2F6F17360
                         722
                                 enyadji.and.e/2.0R.e->e-; IRX
                                  .. PERFORMS THIRD LEVEL PROCESSING
0986
                         723
                                 enyadji.and.0+2.0R.0->0-11RX
0886 4EF2FEF17360
                         724
                         725
                                  .. PERFORMS FOURTH LEVEL PROCESSING
0B8C
                                 enyadj! .and .e + 2 + 2 + 2 + 2 . OR . e
                         726
OBSC 4EF2FEFEFEFEF1
                         727
                                   -> P-JIRX
ØB93 7360
                                  .. PERFORMS FIRST LEVEL PROCESSING
                         728
ØB95
                         729
                                 .. RESULT OF ADJACENCY PROCESSING
0P95
                         730
                                  .. LEFT IN D REGISTER AND AT LOCATION
0895
0P95
                         731
                                  .. ORIGINALLY POINTED TO BY X REGISTER
                                 .. X REGISTER RESTORED TO ENTRY CONDITION
0895
                         732
                                 .. NYADJ REGISTER POINTS TO
0895
                         733
                         734
                                  .. .NOT.DONTWORRY BYTE
0895
0895 D7
                         735
                                 SEP NYMAIN .. RETURN
0896
                                 .. END OF SUBROUTINE ADJPR
                         736
                         737
ØB96
                         738
0B96
                         739
ØB96
                         749
                               ● .. FATAL FAILT LATCHING SECTION, LACHFL
0B96
                                 .. FOR FAULTS WHICH CLOSE DOWN THIS
0P96
                         741
                                 .. SIDE OF SYSTEM
                         742
ØB96
                                 .. NOT A SUBROUTINE, BRANCHED TO WITH
                         743
0B96
                                 .. ERROR CODE NO IN D REGR
                         744
ØB96
                                 .. VALUE OF P VARIES WITH ERROR
                         745
0B96
                                 ORG#BD0
BROB
                         746
                               LACHFL:
ØBDØ
                         747
                                 MARK .. CLOBBERS M(R2)
ØBDØ 79
                         748
                                 SEX R2JIRXIDIS
                         749
0801 E26071
```

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	0BD4		750	DISABLES I/RUPTS, RESTORES X, P
	0BD4	2252	751	DEC R2;->0R2
	ØBD 6		752	RESTORES R2. SAVES ERROR CODE NO
	ØBDA		753	IN ITS CLOBBERED MEMORY LKCN
	08D6	F885AA	754	NY VALW->NY SCR.0
	ØBD9		755	• LACHFL STORAGE LOCK
	ØBD9	F826AF	756	NY VALS->NYH • 0 .
	ØBDC		757	BYTEOOF TIMER
	ØBDC		758	NYH, NYSCR CLOBBERED DOESN'T MATTER
	ØBDC	EA	759	SEX NYSCR
	ØBDD	02734F730F73	760	0R2->0-J0NYH!->0-J0NYH->0-
	0BE3		761	SAVES ERROR CODE NO & TIME
	ØBE3	F823AA	762	NYVALU->NYSCR.0O/P BYTE
F	ØBE6	F800A4	763	A.0(LABLX)->R4.0
Ľ	ØBE9	F800B4	764	A-1(LABLX)->R4-1
	ØBEC	E4D4	765	SEX RAJSEP RA
	OBEE	6442	766	LABLX:OUT4, #42
	arfa	30F0	767	NYLOOP: GO TO NYLOOP
	ØBF2		768	• •L00PS
	0BF2		769	END OF LACHFL, FATAL FAULT LATCHING RE
	ØBF2		770	
	PBF2		771	
	ØBF2		772	END
	ØBF2		774	
	ØBF2	•	775	
В	ØBF2		776	
	08F2		777	END

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FL	LOC	COSMAC CODE		SOURCE LINE
	0000		1	• GSE PROGRAM
	0000		2	•• ENTRY WITH X=R5
	0000		3	P=R7, R5=0C00
	0000		4	
	0000	•	5	TLOC=#03 . ASCII BYTE STORED AT R3
	0000		6	RAM##06DATA SHIFTED FROM R6
	0000		7	
	0000		8	DELAY=#08 . RB 15 DELAY ROUTINE CTR
_	0000		9	OUT=#09 R9 IS O/P ASCII CHAR ROUTINE
•	0000	_	10	••R4 WORKING REG
	0000	(11	CMLOG-#0757
	0000		12	ROMCK=#0750
	0000		13	BDTST=#0792
	0970	•	14	
	0970		15	
	0971	•	16	
_		FAOD	17	
F		C20000	18	
_		FF0:	19	SMI / 01
F	-	C20000	28	** = * · · · · · · · · · · · · · · · · ·
F		FF03C20000	21	SMI #031LBZ RMRNA RAM RETENTION
F		FF01C20000	22	
		FF03C20757	23	
_		FF01C20750	24	
F		FF03C20000	25	
		C00792	26	
	0998	· -	27	
		6450	28	
		3098	29	
		FBFFA5	30	
	09A0	· -	31	7
	39A1		32	
		3AA0	33	
	09A4	- :	34	
	-	6410	35 36	
	-	30A7 F80 0 55	37	
			38	
•	09AC		39	
e	Ø9 AD	8 6F 4A 6	40	
			41	
		6085 3AAE	42	
	_		43	GLO R6
	09B5		43	
		FF80	45	
F	0988	3A00	46	
P		6450	47	
		308D	48	
		6410	49	
	W70F	0410	47	

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```
09C1 30PD
                            50
                                  FF TIME
                                  RMTR:LDI #0A
  09C3 F80A
                            51
  09C5 B9
                            52
                                   PHI R9
                                   LDI #B1;PLO R9; SEF R9..RAM TEST&RESET
  09C6 F8B1A9D9
                            53
                                   SEX R7
  09CA E7
                            54
                                    OUT 4,#10..GSE 1 HIGH SIGNIFIES
  09CB 6410
                            55
                                    · · COMPLETE
  09CD
                            56
  09CD 30CD
                            57
                                  SELF: BR SELF
                                   .. N.B. IF BAD RAM TEST
  09CF
                            58
                                   .. LACHFL PUTS GSE2 HIGH
  09CF
                            59
                            60
                                   .. OUTPUT RAM TO GSE ROUTINE
  09CF
                                  DATOT:LDI#0C
  09CF FB0C
                            61
                                  PHI RAM . . REGISTER DENOTED BY&
                            62
  09D1 B6
                                   LDI#00 . . RAM= 0C00
  09D2 F800
                            63
                                   PLO RAM
  09D4 AK
                            64
  09D5 A4
                            65
                                   PLO WORK . . REG DENOTED BY
                                   .. WORK = XX00
  09D6
                            66
  9906 F800A9
                                   A.0(0PASCI)->R9.0
                            67
                                   A.1(OPASCI)->R9.1
  09D9 F800B9
                            68
  MODC FRAGAS
                            69
                                   A.0(DELRT)->R8.0
                            70
                                   A.1(DELRT)->R8.1
  09DF F80088
  09E2 F821B3
                            71
                                   LDI#21/PHI TLOC
                                   SEP OUT .. TRANSMIT!
  09E5 09
                            72
                            73
                                   LDI#4D;PHI TLOC
  09E6 F84DB3
  09E9 D9
                            74
                                   SEP OUT . "M
                            73
                                   LDI#341PHI TLOC
  09EA F83483
                            76
                                   SEP OUT ... 4
  09ED D95
                                    LDI#34;PHI TLOC; SEP OUT .. "4
  09EE F834B3D9
                            77
                                    LDI#30;PHI TLOC; SEP OUT .. "O
  09F2 F830B3D9
                            78
                                    LDI#30; PHI TLOC; SEP OUT .. "O
                             79
  09F6 F830P3D9
                                    LDI#18; PLO RD...SET FOR 24 SPACES
  09FA FRIBAD
                            80
                                  PHS:LDI#20; PHI TLOC; SEP OUT
  09FD F820E3D9
                            81
                                    DEC ROJALO ROJLBNZ PHS
  ØAØ1 2DBDCAØ9FD
                            82
  0A06 72
                                  READ: LDXA . . READ LOCATION OCOO
                            83
  9497
                            84
                                   .. AND ADVANCED
                             85
                                  PHI WORK
  0A07 B4
                                   SHRISHRISHRISHR
  BABS FAFAFAFA
                            86
  ØAØC FCF6
                             87
                                  ADI#F6
  0A0E 3B00
                            88
                                  BNF LAB 1
                             89
  8A18 FC87
                                  ADI#07
                                   LABI: SMI#C6 . . CONVERT THE FOUR MOST
  OA12 FFC6
                             90
                             91
                                         PHI TLOC .. SIGNIFICANT BITS
  0A14 B3
                                                   .. TO ASCII
                             92
  0A15
                                        SEP OUT .. O/P ASCII BYTE
  9A15 D9
                             93
                                        GHI WORK
   0A16 94
                             94
                             95
                                    SHLISHLISHLISHL
   OA17 PEFEFEFE
                                   SHRI SHRI SHRI SHR
   BAIR FAFAFAFA
                             96
   ØAIF FCF6
                             97
                                     ADI#F6
                             98
                                     BNF LAB 2
F 0A21 3800
                             99
                                    ADI#07
   0A23 FC07
```

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	MA25 FF	FC <i>6</i>	100	LAB2: SMI#C6 CONVERT THE FOUR LEAST
	ØA27 B	3	101	PHI TLOC SIGNIFICANT BITS
	ØA28		102	TO ASCII
	ØA28 D9	· ·	103	SEP OUT O/P ASCII BYTE
	ØA29 F8	300FF	104	LDI#00;SHL · · IS DF=0
	ØA2C 8.		105	GLO WORK
	MA2D FO	C01A4	106	ADI#013PLO WORK CHECKSUM TO STOP G
	0A30 C	80A06	107	LBNF READ. AFTER 256 BYTE TRANSFER
	P433 F8	BODES	108	LDI#0DJPHI TLOC LOAD CRG. RTN.
	ØA36 09	9	109	SEP OUT - TRANSMIT" CARRIAGE RETURN"
	0A37 F	7	110	SEX R7
	0A38 6	410	111	OUT 4.#10ISSUE GSE 1 FLAG
	ØA3A C		112	THIS:LBR THIS
	ØA3D		113	O/P ASCII CHARACTER ROUTINE
	MASD D		114	START: SEP R7
	DASE FE		115	OPASCI:LDI#08;PLO TLOC
	0A41 F		116	LDI#A03PLO TEMP
	8944 TE		117	SEQ
	0A45 D8		110	RETURN: SEP DELAY
	0A46 2		119	DEC TLOC
	9A47 8		120	GLO TLOC
F	0A48 3	200	121	BZ PAREND
	0A4A 9	3	122	GHI TLOC
	0A48 F	-	123	SHR
	MAAC B		124	PHI TLOC
F	0A40 31	BØØ	125	BNF TOM
	0A4F 1	1	126	INC TEMP
	0A50 7	A	127	REQ
	ØA51 38	8	128	SKP
	0A52 7	B	129	TOM: SEQ
	ØA53 C	00A45	139	LBR RETURN
	0A56 8	1	131	PAREND: GLO TEMP
	0A57 F		138	SHR
F	## ## 31	PØØ	133	BNF BILL
	0A5A 7		134	REQ
	ØA5B 3		135	SKP
	ØA5C 7			BILL: SEG EVEN PARITY
	MASD DO		137	SEP DELAY
	BASE 7		1 38	REQ
	ØASF D		139	SEP DELAY
	MAKE DE	8	1 40	SEP DELAY
	ØA61 C	00A3N	141	LBR START
	BAKA		1 42	DELAY ROUTINE
	0A64 D		1 43	STRIISEP R9
	MAKS FI	·· · ·		DELRT:LDI#51 FOR 300 BAUD
	0A67 F		1 45	DIL:SMI #01
	9869 C	•	1 46	NOPINOP
	DAGE 3	-		BNZ DIL
	OAGD C	00A64	-	LBR STRI
	0A70		1 49	• • • BOARD TEST PROGRAM

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```
... (GSE SWITCH AT B'111'
0A70
                         150
0792
                         151
                                ORG#0792
0792 F890
                                LDI#90
                         152
                                PLO RE
0794 A2
                         153
0795 F800B1R9
                                A.1(INADR)~>R1.1,R9.1
                         154
0799 F800A1
                         155
                                A-0(INAOR)->R1.0 .. INTERRUPT ADDRESS
079C E7
                         156
                                SEX R7
079D 7077
                                RET, A77
                         157
079F F800A9
                         1 58
                                A.0(DALLY)->R9.0
07A2 FS61D962D9
                         159
                                SEX RSJOUT 1JSEP R9JOUT 2JSEP R9
07A7 63D964D967D9
                         160
                                OUT 31SEP R91OUT 41SEP R91OUT 71SEP R9
07AD C00200
                                LPR #0200
                         161
0780 7A
                               CMBAK: REQ
                         162
07R1 F800A5
                         163
                               CIRCLE: LDI#00; PLO R5 .. TO RESET PORT
0784 3400F80155
                                B1 HAYJLDI#0135TR R5
                         164
0789 3500F802F155
                         165
                               HAY: B2 BEE; LDI#02; OR; STR R5
07BF 3600F804F155
                               BEE: B3 SEAJLDI 4; OR; STR R5
                         166
07C5 3700F808F155
                         167
                               SEA:B4 DEE;LDI B;OR;STR R5 -
07CP 64
                         168
                               DEE:OUT 4
07CC 30B1
                         169
                                BR CIRCLE
Ø7CE D7
                               PIE:SEP R7
                         170
07CF FBAORFAF
                         171
                               DALLY:LDI#A@;PHI RF;PLO RF; .. APPROX
                               HONEY: DEC REJGHI REJENZ HONEY
07D3 2F9F3AD3
                         172
0707
                         173
                                                             · · I S DELAY
07D7 30CE
                                BR PIE
                         174
07D9
                         175
                                ORG* . . . . DOES NOTHING! !
0709 6072FE7270
                         176
                               BYBYE: IRXILDXA; SHLJLDXA; RET
                                INADRIDEC REISAVIDEC REISTXD
070F 22782273
                         177
                                                                .. SAVE ACC
Ø752 7673
                                 SHRC: STXD .. SAVE DF
                         178
                               LDIWARJPHI REJPLO REJSEQ
07E4 FBA0BEAETR
                         179
                               CRAZY: DEC REJGHI REJANZ CRAZY .. 1 SEC DE
07E9 2E9E3AE9
                         180
07ED 7A30D9
                         181
                                REQ; BR BYBYE
                                 ORG#0200; SEO; SEP R9; LBR#05F9
0200 7BD9C005F9
                         182
                                 ORG#05F9; PED; SEP R9JLBR#078D
MSF9 TANGCHMTAD
                         183
                                 ORG#078D; SEN; SEP R9; LBR#0968
078D 78D9C00968
                         184
                                 ORG#00 68; REQ; SEP R9; LBR#0AF1
0968 7AD9C00AF1
                         185
                                 ORG#ØAFIJSEQJSEP R9JLBRCMBAK
ØAF1 7809CØØ78Ø
                         186
                                 .. THESE ARE SKIP THROUGH
ØAF6
                         187
ØAF6
                         188
                                 .. ADDRESSES TO PROVE
0AF4
                         189
                                 .. MEMORY DECODING IS OK
```

```
0000 1
                    (min1
                           .. +++++COMMON LOGIC TEST PROGRAMME+++++
0000 1
                    0002 DRG00757
0257 E74
                    0003 SEX R7
0758 6200;
                    0004 BUT 2,000
                    0005 NOP NOP
                                  .. AM I MASTER
075A: 04041
0750 200
                    0006 DEC RO
075D E0;
                    0007 SEX PO
075E F0FA02;
                    0008 LDX ANI#02
0761 E74
                    0009 SEX R7
0762 3270;
                    0010 BZ SLAVE
0764 64043
                    0011 BEGIN: DUT 4,004 .. ISSUE TAS,FIRE & GSE 2
                    0012 LDI#40 PHI R4 PLO R4 ..APPROX 400 MS DELAY
0766 F840R4641
076A 24943A6A:
                    0013 DILI: DEC R4 GHI R4 BNZ DIL1
                    0014 OUT 4,098 .. RESET FIRE & GSE 2, ISSUE
076E 64981
                    0015 LDI#40 PHI R4 PLO R4 .. INHIBIT & GSE 1
0770 F840B4A4;
0774 24941
                    0016 DIL2: DEC R4 GHI R4
0776 3A74;
                    0017 BNZ DILZ .. TIME DELAY
0778 64501
                    0018 FLASH: DUT 4,050 .. RESET INHIBIT, THE &
077A 307A;
                    0019 THIS: BP THIS
                                        ...ISSUE 65E 1 & 2
0770 F8FFB4641
                    0020 SLAVE: LDIOFF PHI R4 PLD R4
0780 2494041
                    0021 DELAY: DEC R4 GHI R4 NOP .. APPROX 2 SEC DELAY
                    0022 BNZ DELAY
0783 3A801
0785 35641
                    0023 SELF: B2 BEGIN
0787 30851
                    0024 BR SELF
0789 ;
                    0025
0789 1
                    9500
0789 4
                            ..... CHECK DET UP+++++
                    7500
0789 4
                    8500
0789 :
                    0029 ORGO0740 .. ROM CHECK SET U.
0740 F823A51
                     0030 SEVENILDIAZU PLO R5 ..ALL REGID SUP
                     0031 LDI#80 STR P5 ..CORPECT SET
0743 F88055;
                     0032 LDIOFF PLO P5 ..UP TO ENTER
0746 F8FFA51
0749 F801B34
                     0033 LDI#01 PHI R3 ..BACKGROUND PGM.
074C F870A3:
                     0034 LDI#70 PLO R3
074F D34
                     0035 SEP R3
0750 30401
                     0036 BR SEVEN ..ENTRY POINT
11752 1
                     0037 DRG#05F9
05F9 7AD900078D1
                    0038 +07A+0D9+0C0+007+08D ..NOT USED IN PROG.BUT LEFT GUSP
05FE :
                    0.039 DR6#0AF1
0AF1 7BD90007B04
                     0040 +#78,#D9,#C0,#07,#80 ..FROM PREVIOUS EDITS
URF6 :
                     0041
                                                  .. AND MUST BE INCLUDED FOR
DAF6 $
                     0042
                                                  .. CORRECT PARITY
NAF6 #
                     0043 END
0000
```

? F, H, L, U=

ţ

APPENDIX A-3

INSTRUCTION SUMMARY FOR 1802

Appendix A — Instruction Summary

The COSMAC instruction summary is given in Tables I and II. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where W=N or X, or P

R(W).0: Lower-order byte of R(W) R(W).1: Higher-order byte of R(W) NO = Least significant Bit of N Register

Operation Notation $M(R(N)) \rightarrow D; R(N) + 1$

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

TABLE I - INSTRUCTION SUMMARY by Class of Operation

Register Operations

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
INCREMENT REG N	INC	1N	R(N) +1
DECREMENT REG N	DEC	2N	R(N) -1
INCREMENT REG X	IRX	60	R(X) +1
GET LOW REG N	GLO	8tN	R(N).0-D
PUT LOW REG N	PLO	AN	D→R(N).0
GET HIGH REG N	GHI	9N	R(N),1→D
PUT HIGH REG N	PHI	BN	D-R(N).1

Memory Reference

INSTRUCTION	MNEMONIC	OP	OPERATION
LOAD VIA'N	LDN	ON	M(R(N))-D; FOR N NOT 0
LOAD ADVANCE	LDA	4N	M(R(N))-D:R(N) +1
LOAD VIA X	LDX	FO	M(R(X))-D
LOAD VIA X AND ADVANCE	LDXA	72	M(R(X))→D; R(X) +1
LOAD IMMEDIATE	LDI	F8	M(R(P))-D:R(P) + 1
STORE VIA N	STR	5N	D→M(R(N))
STORE VIA X AND DECREMENT	STXD	73	D→M(R(X)); R(X) -1

Logic Operations

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
OR	OR	F1	M(R(X)) OR D→D
OR IMMEDIATE	ORI	F9	M(R(P)) OR D-D; R(P) +1
EXCLUSIVE OR	XOR	F3	M(R(X)) XOR D-D
EXCLUSIVE OR IMMEDIATE	XRI	FB	M(R(P)) XOR D-D; R(P) +1
AND	AND	F2	M(R(X)) AND D-D
AND IMMEDIATE	ANI	FA	M(R(P)) AND D-D; R(P) +1
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, LSB(D)-DF
SHIFT RIGHT WITH CARRY	SHRC }	76●	SHIFT D RIGHT, LSB(D)-DF
RING SHIFT RIGHT	RSHR \	1	
SHIFT LEFT	SHL	FE	SHIFT D LEFT, MSB(D)-DF,
SHIFT LEFT WITH CARRY	SHLC]	7E ♦	SHIFT D LEFT, MSB(D)-DF,
RING SHIFT LEFT	RSHL	ì	1

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Arithmetic Operations

INSTRUCTION	MNEMONIC	CODE	OPERATION
ADD	ADD	F4	M(R(X)) +D-DF, D
ADD IMMEDIATE	ADI	FC	M(R(P)) +D+DF, D, R(P) +1
ADD WITH CARRY	ADC	74	M(R(X)) +D +DF+DF, D
ADD WITH CARRY, IMMEDIATE	ADCI	7C	M(R(P)) +D +DF+DF, D
	1 00		R(P) +1
SUBTRACT D	SD	F5	M(R(X)) - D•DF, D
SUBTRACT D IMMEDIATE	SDI	FD	M(R(P)) D+DF, D, R(P) +1
SUBTRACT D WITH	SDB	75	M(R(X))-D-(NOT DF)-DF, D
BORROW			
SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	70	M(R(P)) D (NOT DF)-DF, D;
SUBTRACT MEMORY	SM	F7	D M(R(X)) DF. D
SUBTRACT MEMORY	SMI	FF	D M(R(P)) DF. D.
IMMEDIATE		ŀ	R(P) +1
SUBTRACT MEMORY WITH	SMB	77	D M(R(X))- (NOT DF)+DF, D
BORROW			
SUBTRACT MEMORY WITH	5.181	7F	D-M(R(P))-(NOT DF)-DF, D
BORROW, IMMEDIATE			R(P) +1

Branch Instructions - Short Branch

SHORT BRANCH .	BR	30 38	M(R(P))+R(P).0
NO SHORT BRANCH (SEE SKP)	NBR	38*	R(P) +1
SHORT BRANCH IF D=0	BZ	32	IF D=0, M(R(P))-R(P).0 ELSE R(P) +1
SHORT BRANCH IF D NOT 0	BNZ	3A	IF D NOT 0, M(R(P))-R(P).0 ELSE R(P) +1
SHORT BRANCH IF DF+1	80F		
SHORT BRANCH IF POS OR ZERO	BPZ	33€	IF DF+1, M(R(P))+R(P).0 ELSE R(P) +1
SHORT BRANCH IF EQUAL	BGE)	1	
OR GREATER SHORT BRANCH IF DF-0	BNF)	38	IF DF-0, M(R(P))-R(P).0
SHORT BRANCH IF MINUS	BM }	1 30	ELSE R(P) +1
SHORT BRANCH IF LESS	BL)	i	
SHORT BRANCH IF Q-1	BQ	31	IF Q=1, M(R(P))-R(P).0 ELSE R(P) +1
SHORT BRANCH IF O-0	BNO	39	IF Q -0, M(R(P))-R(P) 0 ELSE R(P) +1
SHORT BRANCH IF EF1-1	81	34	IF EF1 1, M(R(P))+R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF1-0	BN1	3C	IF EF1=0, M(R(P))+R(P).0 ELSE R(P) +1
(0 - VCC) SHORT BRANCH IF EF2:1 (1 VSS)	82	35	IF EF2=1, M(R(P))+R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF2-0	BN2	3D	IF EF2=0, M(R(P))-R(P) 0 ELSE R(P) +1
SHORT BRANCH IF EF3=1	83	36	IF EF3-1, M(R(P))+R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF3=0	BN3	3E	IF EF3=0, M(R(P))+R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF4-1	B4	37	IF EF4=1, M(R(P))+R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF4=0	BN4	3F	IF EF4 0, M(R(P))-R(P).0 ELSE R(P) +1



Branch Instructions - Long Branch

INSTRUCTION	MNEMONIC	OP	OPERATION
LONG BRANCH	LBR	CO	M(R(P))→R(P).1 M(R(P)+1)→R(P).0
NO LONG BRANCH (SEE LSKP)	NLBR	C 8 ●	R(P) +2
LONG BRANCH IF D=0	LBZ	C2	IF D=0, M(R(P))→R(P).1 M(R(P)+1)→R(P).0
LONG BRANCH IF D NOT 0	LBNZ	CA	ELSE R(P) +2 IF D NOT 0, M(R(P))→ R(P).1 M(R(P) +1)→ R(P).0
LONG BRANCH IF DF-1	LBDF	C3	ELSE R(P) +2 1F DF=1, M(R(P))→R(P).1 M(R(P) +1)→ R(P).0
LONG BRANCH IF DF=0	LBNF	св	ELSE R(P) +2 IF DF=0, M(R(P))→R(P).1 M(R(P) +1)→ R(P).0
LONG BRANCH IF Q=1	LBQ	C1	ELSE R(P) +2 IF Q=1, M(R(P)) \rightarrow R(P).1 M(R(P) +1) \rightarrow R(P).0 ELSE R(P) +2
LONG BRANCH IF Q=0	LSNO	C9	IF Q=0, M(R(P))→R(P).1 M(R(P) +1)→ R(P).0 ELSE R(P) +2

Skip Instructions

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
SHORT SKIP (SEE NBR)	SKP	38	R(P) +1
LONG SKIP (SEE NLBR)	LSKP	C8 ⁴	R(P) +2
LONG SKIP IF D=0	LSZ	CE	IF D=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF D NOT 0	'.SNZ	C6	IF D NOT 0, R(P) +2 ELSE CONTINUE
LONG SKIP IF DF=1	LSDF	CF	IF DF=1, R(P) +2 ELSE CONTINUE
LONG SKIP IF DF-0	LSNF	C7	IF DF=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF Q=1	LSQ	CD	IF Q=1, R(P) +2 ELSE CONTINUE
LONG SKIP IF Q=0	LSNO	C5	IF Q=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF IE=1	LSIE	СС	IF IE=1, R(P) +2 ELSE CONTINUE

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Control Instructions

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
IDLE	IDL	00	WAIT FOR DMA OR INTERRUPT; M(R(0))-BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N→P
SET X	SEX	EN	ÌN→X
SET Q	SEQ	78	1-Q
RESET O	REQ	7A	0-Q
SAVE	SAV	78	T→M(R(X))
PUSH X,P TO STACK	MARK	79	(X,P)→T; (X,P)→M(R(2)) THEN P→X: R(2)-1
RETURN	RET	70	M(R(X))→(X,P); R(X) +1
DISABLE	DIS	71	M(R(X))→(X,P); R(X) +1 0→1E

Input-Output Byte Transfer

MNEMONIC	OP CODE	OPERATION
OUT 1	61	M(R(X))→BUS; R(X) +1;
1	}	N LINES = 1
OUT 2	62	M(R(X))→BUS; R(X) +1;
		N LINES = 2
) OUT 3	63	M(R(X))→BUS; R(X) +1;
OUTA		N LINES + 3 M(R(X))→BUS; R(X) +1;
0014	04	N LINES = 4
OUTS	66	M(R(X))→BUS; R(X) +1;
1	"	N LINES = 5
OUT 6	66	M(R(X))-BUS; R(X) +1;
	ł	N LINES = 6
OUT 7	67	M(R(X))→BUS; R(X) +1;
1 1010 4		N LINES = 7
INP	OA	BUS-M(R(X)); BUS-D; N LINES = 1
1610 4	; RA	BUS→M(R(X)): BUS→D:
11	. 0-	N LINES = 2
INP 3	ં ઠઉ	BUS-M(R(X)):BUS-D:
		N LINES = 3
INP 4	6C	BUS→M(R(X)); BUS→D;
1	i	N LINES = 4
INP 5	60	BUS→M(R(X)); BUS→D;
		N LINES - 5
INP	l er	BUS→M(R(X));BUS→D;
1849 7	AE	N LINES = 6 BUS-M(R(X)), BUS-D;
in /	OF .	N LINES = 7
	OUT 1 OUT 2 OUT 3 OUT 4 OUT 5 OUT 6 OUT 7 INP 1 INP 2	MNEMONIC CODE OUT 1 61 OUT 2 62 OUT 3 63 OUT 4 64 OUT 5 65 OUT 6 66 OUT 7 87 INP 1 89 INP 2 6A INP 3 60 INP 5 6D INP 6 6E

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APPENDIX A-4

COSMAC LEVEL 2 ASSEMBLY LANGUAGE

CUSMAC Level 11 Assembly Language

In order to make programming easier, in Level II operations several of the op-code mnemonics can be replaced with codes that correspond to their most frequent use. Likewise, operations involving the D register can be done using D-sequence instructions. In D-sequence instructions, special characters are used instead of op-code mnemonics making D-sequence instructions similar in appearance to APL statements. (APL is a high-level. programming language)

Executable Statements: Level II

Substitution Instructions. The substitutions for the op-code mnemonics fall into two forms. The mnemonics and their substitutions are listed in Table VI. The first form involves simply the use of an immediate keyword in the same way that the mnemonic was used. These keywords are IDLE, GOTO, NOGOTO, SKIP, RETURN, DISABLE, POP, PUSH, SAVE, GOSTATE, CALL, and EXIT. EXIT is treated like a first class instruction and CALL is treated like a macro call in that it is followed by an operand string. They are used to execute the standard call and return procedures. In order to use them, the registers 2 through 6 must already be set aside for the standard call and, return procedure. They can be initialized by using the Utility Program UT21 built—in subroutines, INIT1 and INIT2. (Refer to Chapter 10). The operands of CALL consist of the address of the subroutine, followed by any inline parameters that the programmer wishes to pass. EXIT has no operands.

The second form consists of the word IF followed by a space, a BRANCH keyword, another space, and the keyword GOTO. The BRANCH keywords indicate the condition on which a branch is to take place. They are Q, 4-, -0, DF, PZ, GE, EF1, EF2, EF3, EF4, NQ, 6>0, NDF, MINUS, LESS, NEF1, NEF2, NEF3, and NEF4.

<immediate Payword> := IDLE|GOTO|NOGOTO|SKIP|RETURN
|DISABLE|POP|PUSH|SAVE|GOSTATE|CALL|EXIT

<br

Examples:

IDLE IDL GOTO ADD NUMS BR ADD NUMS IF -U COTO BEGINNING BZ BEGINNING BN4 END IP NEP4 GOTO END_ GOSTATE RS SEP R5 CALL TYPE, 'MESSAGE' SEP R4 DC TYPE DC 'MESSAGE' PUSH X STXD X POP Y LDA Y

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D-Sequence Instructions. The D-Sequence instructions consist of three parts, the load part, the manipulation part, and the storage part. What each of these parts corresponds to is listed in Table VII. Not all parts are needed in a statement. Any single part can be present or all can be present. Two parts can also be present, but if more than one part is present, the order load, manipulation, and storage part must be maintained.

The load part tells the assembler what should be loaded into the D-register. A register name followed by a .0 or .1 indicates the either the low- or high-order byte of that register should be loaded into D. A constant, identifier, or term in parentheses indicates that the value of that constant, identifier, or term should be loaded immediately into the D-register. An @ indicates that the D-register should be loaded from memory. If a register name follows the @, then the byte pointed to by that register is used. If no register name is specified, the register named by the X register used. If a "precedes the register name it indicates that the X-register should be set to point to that register. If memory is accessed and a ! ends the load part, the contents of the register used is incremented. If the @ ends the load part, a comment in parentheses may be inserted immediately (without spaces) after the @.

The manipulation part tells the assembler what is to be done with the D-register. There are 9 binary operations which can be performed and 4 unary operations. The binary operations are + (add), - (subtract), -+ (subtract and negate), +" (add with carry), -" (subtract with borrow), -+" (subtract and negate with borrow), .AND. (and), .OR. (or), and .XOR. (exclusive or). The manipulation part for the binary operations consists of the operator symbol followed without spaces by the source of the second operand. The source can be a memory location, a constant, an identifier, or a term in parentheses. If a constant, identifier, or term is used, its value is immediately used. To use the memory, an @ immediately follows the operation symbol. Immediately following the @ there is a " followed by a register name. The X-register is set to register name and the register points to the memory byte that is used. The unary operators are /2 (shift right), *2 (shift left), /2" (shift right circular) or *2" (shift left circular).

The storage part tells the assembler what to do with the contents of the D-register. All storage parts begin with -> (a minus followed by a greater than). If a register name followed by .0 or .1 follows the arrow (->), the contents are stored in the low- or high-order byte of that register. If an 0 follows the arrow, the contents are stored in memory. If a register name follows the 0, it points to the byte in memory where the D-register contents are to be stored. If no register name follows the 0, the register specified by the X-register is used. The 0 may be followed by a - indicating that the contents of the register used should be decremented. If the - is used, then the register name (if there is one) must be separated from the - by a ". The X-register is set to the register name given. If the 0- is the end of the storage part, then a comment within parentheses may immediately follow the 0-.

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Note that no spaces are allowed between the special characters involved or between the special characters and any identifiers or registers that are used. There is also a limit on the length of a Level II statement. It may be contain no more than thirty-nine characters.

Examples:

5->R5.0 LDI 5;PLO R5
5 LDI 5
LDI A
FIVE+2->R7.0 LDI FIVE;ADI 2;PLO R7
QN!->Q-"N LDA N;SEX N:STXD
.XOR.CAR RET
(FIVE+SIX)->QUTILITY LDI 11:STR UTILITY

Sample Program Illustrating D-Sequences. Fig. 13 is a repeat of Fig. 12 thefirst sample program written in Level II assembly. It illustrates the use of the D-sequence statements and substitutions.

Table VI - Level II Substitutions for Level I Mnemonics

Level I	Level II
Bl	IF EF1 GOTO
B2	IF EF2 GOTO
83	if ef3 coto
В4	IF EP4 GOTO
BDF	IF DP GOTO
BGE	IF GE GOTO
BL	if less cuto
BM	IF HINUS GOTO
BN1	IP NEFI GOTO
BN2	IF NEF2 GOTO
BN3	if nef3 goto
BN4	ip nep4 goto
BNF	IF NDF GOTO
BNQ	IF NQ GOTO
BNZ	IF 4>0 GOTO
	IF >0 GOT"
BPZ	IF PZ GOTO
BR	GOTO
BQ	IF Q GOTO
BZ	IF 4=0 GOTO
	IF -0 GOTO
DIS	DISABLE
IDL	idle
LDXA	POP
NBR	NOGOTO
ret	RETURN
SAV	SAVE
SEP	COSTATE
SKP	SKIP
STXD	PUSH
SEP R4	CALL
SEP R5	EXIT

Table VII - D-Sequence Statements

Symbol	lavel I	Action		
Load Part				
0	LUX	M(R(X))->D		
@"n	SEX N:LDX	N->X; M(K(X))->D		
@(COMMENT)	LDX COMMENT	M(K(X))->D		
@N	LDN N	M(R(N))->D FOR N<>0		
N.O	GLO N	R(N).0->D		
N.1	GHI N	R(N).1->D		
e n 1	LDA N	m(R(N))->D;R(N)+l->R(N)		
CONST ANT	LDI CONSTANT	A.O(CONSTANT)->D		
e 1	LDXA	M(R(X))=>D;R(X)+1=>R(X)		
Manipulation Part				
+@	ADD	D+M(R(X))->DF,D		
+@"N	SEX N; ADD	N->X;D+M(K(X))->DF,D		
+CONSTANT	ADI CONSTANT	D+CUNSTANT->DF,D		
-@	SM	D-M(R(X))->DF,D		
-e~n	SEX N; SM	N->X;D-M(R(X))->DF,D		
-CONSTANT	SHI CONSTANT	D-CONST ANT->DF , D		
-+0	SD	M(R(X))-D->DP,D		
@"N	SEX N;SD	$N->X;M(R(X))\sim D->DF,D$		
-+ CONSTANT	SDI CONSTANT	CONSTANT-D->DF,D		
+"6	ADC	D+M(R(X))+DF->DF,D		
+"@"N"	SEX N; ADC	$N->X;D+M(R(X))+DF->DF_D$		
+"CONST ANT	ADCI CONSTANT	D+CONST ANT+DF->DF,D		
 @	SMB	D-M(R(X))-NDF->DF,D		
0"N	SEX N;SMB	N->X;D-M(R(X))-NDF->DF,D		
-"CONSTANT	SMBI CONSTANT	D-CONSTANT-NUF->DF,D		
→ "@	SDB	M(R(X))-D-NDF->DF,D		
→"@"N	SEX N; SDB	N->X;M(R(X))-NDF->DF,D		
→"CONSTANT	SDBI CONSTANT	CONSTANT-D-NDF->DF,D		
.AND.@	AND	D.AND.M(R(X))->D		
.And.e"n	SEX N; AND	N->X;D.AND.M(R(X))->D		
.AND.CONSTANT	AN I CONSTANT	D.ANG.CONSTANT->D		
.OR.@	OR	$D.OR.M(R(X)) \rightarrow D$		
.or.@"N	SEX N; OR	N->X; D.OR.H(R(X))->D		
OR. CONSTANT	OR1 CONSTANT	D.OR.CONSTANT->D		
.xor.@	XOR	$D.XOR.H(R(X)) \rightarrow D$		
.xor.@"n	SEX N; XOR	N->X;D.XOR.M(R(X))->D		
.XOR.CONSTANT	XRI CONSTANT	D.XON.CONSTANT->D		

Table VII (cont'd)

Symbol	Level I	Action
Manipulation Pa	irt	
/2	SHR	SHIFT D RIGHT NONCIRCULAR
* 2	SHL	SHIFT D LEFT NONCIRCHIAR
/2"	SHRC	SHIFT D RIGHT CIRCULAR
*2"	SHLC	SHIFT D LEFT CIRCULAR
Storage Part		
->N.O	PLO N	D->R(N).0
->N.1	PHI N	D->R(N).1
->@N	STR N	D->M(R(N))
->(9-	STXD	D->M(R(X));R(X)-1->R(X)
->@-"N	SEX N;STXD	N->x; D->M(R(X)); R(X)-1->R(X)
->e-(comment)	STXD COMMENT	$D\rightarrow M(R(X));R(X)=1\rightarrow R(X)$

Note I: Wherever an N appears, a register may be placed. (R followed by a hexadecimal digit or a hexadecimal constant less than IOH)

Note 2: Wherever the word constant appears, a constant or valid identifier may be placed.

Note 3: Wherever an θ appears at the end of a part (not followed by "N, N, or 1), it may be replaced with θ (comment).

APPENDIX B-1

3

QUALITY DATA SHEETS - Q5304 Q5308 Q5309 Q5310 THE:

DRAFT ACCEPTANCE REQUIREMENTS FOR 53521-012
AND 53522-011 HIGH TEMPERATURE U.V. DETECTORS
PART A. MANDARONT MEMOTERALIMETS

DEFINITION

becomes a master deciment for function performance testing of U.V. Detectors.

Performance values have been defined in compliance with "funnel" or "tiered telerances" shibscophy and form the following extensives.

Type 1 - Fectory or Production Acceptance Limits
especiate at nerval authient temperature conditions.

Type 2 - Receiving Inspection or Customer Acceptance Limits
assessible at normal emblant temperature conditions.

Type 3 - Quality or Functional Acceptance Limits appropriate at and between the declared extremes of appropriate temperature.

in any repeat of test in two geographical areas there is expected to be some difference in test results. Differences within the stated accuracy of instrumentation and those due to acceptable variances based upon time dependency, transportation and test techniques are declared as acceptable. To meet these circumstances Type 1 limits used for Factory tests allow a smaller variation that these used for Type 2 limits by Receiving Inspection and as Customer Acceptance. These tests are carried out at normal ambient temperature conditions.

Functional limits at extremes of operating conditions are determined and declared. From time to time quality audit tests may be carried out and performance characteristics are measured for compliance with values of the approval sample which are measured at appropriate extreme conditions, particularly with respect to temperature. Type 3 limits cater for functional acceptance characteristics and allow a greater variation than Type 2 limits.

The correct acceptance value applicable to the nature of the test is detailed in a schedule and is to be selected for use as appropriate. Any specified test where a single value remains in the test is applicable to Type 1, 2 and 3 tests.

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						orsonnel's e ₎ Soler Lemp		. rediction	from	emitters on		
1.	IDENT	FICA	TION	<u> </u>								
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2.	FREQU	ENC	Y OF	TEST								
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GRAVINER LIMITED, COLNBROOK ENGLAND

SHEET No.

QUALITY CONTROL DATA SHEET

SHEET No.

No. OF SHEETS

TITLE:

DRAFT ACCEPTANCE REQUIREMENTS FOR 53521-012 AND 53522-011 HIGH TEMPERATURE U.V. DETECTORS PART, A. MANDATORY REQUIREMENTS.

5.1.1. Calibration of Test Equipment

The U.V. source shall satisfy the following requirements:-

When measured at the front face of the U.V. Detector, irradiance at wave length 220 nm and bandwidth less than 10 nm shall not be prester than 3 x 10-10 watts/cm².

Irradiance at any other wavelength between 270 and 320 nm of a bandwidth less than 10 nm shall not be greater than 10⁻⁷ watts/cm².

A 5" see fire at a distance of 4 ft. satisfies this requirement.

The standard test emitters (type 45666-201) mounted on the test equipment (Tool No. 697-128), shall be calibrated, to give the same output response from the reference photocell, as when that photocell views the above pan fire.

This calibration is additional to the pre-checking calibration Note: required by the test procedure.

5.1.2. Test Sequence

The following tests shall be performed in sequence.

5.2. Sensitivity

The calibrated photocell shall be mounted in the Test Kit, Tool No. 697-128. the positive terminal in the A+ position. The applied voltage shall be 320V - 5v.

The count rate from the reference photocell shall be used in conjunction with Table 1 to compute the radiation falling on the photocell, and the acceptance value for the detector head on test.

5.2.1. Sensitivity as a Function of Gas Leakage

The applied voltage of the cell on test shall be reduced to ~ (See 5.6.)

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		NTROL DATA SHEET	SHEET No.	4	No. OF SHEETS			
Œ:	AND 535	CCEPTANCE REQUIREMENTS FO 22-011 HIGH TEMPERATURE U. NANDAPORT REQUIREMENTS.						
	5.2.1.	Sensitivity as a Function of Go	s Leakage (cont	d.)				
		The voltage to test emitter shall be switched Off.						
		After a minimum period of 5 se switched on.	conds, the test of	emitte	r shall be			
		The count rate from the detects 5 pulses/sec.	or on test shall b	e gre	ater than			
5.3.	Solor Immun.,							
	With a supply voltage of $320V \stackrel{+}{-} 5V$ applied, the detector on test shall be exposed to a solar lamp (697-112). The electrodes of the cell shall be $2.5" \stackrel{-}{-} 0.25"$ from the lamp filter.							
	The count rate shell be less than - (See para. 5.)							
5.4.	U.V. Emitter Test							
	5.4.1.	Law Voltage Operation						
		The voltage shall be set to make the switched on, and the dischadarrows the narrows gap of the than 30 seconds.	arge of the er th	er obs	erved to occur			
	5.4.2.	High Voltage Operation						
		The applied voltage shall be so be switched on and the dischar narrowest gap of the electrodes 30 seconds.	ge observed to d	CCUT	across the			
5.5.	Insulation Test							
		plation between the live pins link not less than 20 magnins, et 50		id the	detector case			

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GRAYINER LIMITED, COLNERCOK, ENGLAND	SHEET No.	△ 5304
QUALITY CONTROL DATA SHEET	SHEET No.	No. OF SHILETS

TITLE: DRAFT ACCEPTANCE REQUIREMENTS FOR 53521-012
AND 53522-011 HIGH TEMPERATURE U.V. DETECTORS

PART A. HANDAPORT HEQUINERIESTS.

5.6. Schedule of Test Limits

Test Definition	Category	Value	Unit
5.2.1.	1	280	Volts
	2	285	. Yolfs
	3	290	Volts
5.3.	1	1.2	Pulses/sec.
	2	5	Pulsos/sec.
	3	5	Pulses/sec.
5.4.1.	1	280	Volts
	2	285	Volts
	3	290	Volts

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GRAVINER LIMITED, COLNEROOK, ENGLAND.	Jaurei 140		5304
QUALITY CONTROL DATA SHEET	SHEET No.	وا	No. OF SHEETS

TITLE: DRAFT ACCEPTANCE REQUIREMENTS FOR 53521-012
AND 53522-011 HIGH TEMPERATURE U.V. DETECTORS

PART A. MANDATORY MEQUIREMENTS.

TABLE 1

CHANNEL B	PROBE ACCEPTANCE
TEST EMITTER	COUNT RATE (PULSE/SEC)
1.49	68
1.3y	63
1.2y	58
1.ly	53
У	48 •
0.9y	43
0. 8 y	38
0.7y	33
0. 6 y	28

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GRAYMER LIMITED, COLNEROOK, ENGLAND.

OUALITY CONTROL DATA SHEET

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OUALITY CONTROL DATA SHEET

TITLE:

DRAFT ACCEPTANCE REQUIREMENTS FOR \$3\$21-012
AND 53522-011 HIGH TEMPERATURE U.V. DETECTORS
PART B. CHAVINEN PREPERED TEMPINO PROGRESSES.

1. EQUIPMENT REQUIRED

Test Kit - 697-128.
Test Kit to detector head adaptor.
Calibrated photocell
Pulse counter with 100 sec. gate times
Solar Lamp - Tool No. 697-112 and 2 filters.
D.V.M. with D.C. 1 KV range.

2. SETTING UP PROCEDURE FOR CALIBRATION

S1 and S3 to OFF.

\$2 to position B.

S4 to position B+

S5 to position 3

Só to position 1.

S8 to position OUT.

S7 to position 2.

Connect SNC 1 to pulse counter and SKT? to DVM.

Set counter to DC Channel A.

Set pulse counter to 100 sec. gate.

Set D.V.M. to suitable range (more than 3200)

59 to 2 mS.

3. CALIBRATION PROCEDURE

Fit calibrated photocell to test kit with positive pine to position A, when keeps and holder is in B position.

51 to position ON. LPI will illuminate. Allow 5 r res worm up time.

D.V.M. to read 320V = 5V, S8 to position IN.

53 to position ON, test emitter B will illuminate.

Press reset button on pulse counter.

At the end of 100 second period, total counts will be unsplayed. These, $\cos t$ in conjunction with the collibration cortificate and Table 1, ascertain the accuprance level to be used.

\$3 to OFF when counts are displayed

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TITLE:	-	ND 53	522-011	HIGH	TEMPE	RATUR	EU.V.	53521-0 DETECTO CEDURE.	12 ORS		
4.	SETTI	NG UF	PROCE	DURE F	OR TE	STING					
	S) an	d S3 to	OFF.								
	-	positio									
		positio									
		positio		•							
		poritio	n I. n CUI.								
		positio									
	59 to	positio	n 2 mS.								
	Adop	ter swil	ches to	position	P/Col	l and p	coltion	A. 	hian a-		base bit
	Conn	ect ada	ptor to	test Kil	n con	noct ic	d. Fish	p to cart	ming po	with ah	otocell in line
	with	emitter	8. In 1	he ones	of a d	uol hes	d, alig	n P/Cell	A with	emitte	7.
5.	SENS	ITIVIT	Y TEST								
	5.1.	Sing	ie Head	, and C	hannel	A of C	ual Hea	rd_			
		51 N	positio	n ON,	LP] w	ill ilhon	inote.				
			.M. to		SV = 5	٧.					
			o positio			:11 :41.	:				
		5J N	ON,	lest emi	mers v	counts	minare. The	cou nts w	م مط الن	ecorde	d after 100 secs.
			r to eco								
		53 M	o Off a	fler cou	ants how	ve been	records	od.			
		CI.		C D1	L4						
	5.2.	Cha	nne! B o	1 0001	1000						
		Swit	ch on A	daptor	to B.						
		Allig	n photo	cell B v	rith tos						
			ON.								d after 100 secs
			s reset o or to acc					COUNT W	/III 54 /		
			o Off c					ed.			
ISSU	E	Δ			Γ	<u> </u>					T
MO	D							1			
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API					1	†- 	}				-

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DATA SHEET No. Q 5304

SHEET. No.

QUALITY CONTROL DATA SHEET

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No. OF SHEETS

TITLE:

DRAFT ACCEPTANCE REQUIREMENTS FOR 53521-012
AND 53522-011 HIGH TEMPERATURE U.V. DETECTORS
PART &. QUAVIDER PREFEMED TESTING PROCESSINE.

6. SENSITIVITY AS A FUNCTION OF GAS LEAKAGE

6.1. Channel B (Dual Head)

S8 to position OUT.

S7 to position 4.

D.V.M. to read 280V - 5V.

S8 to IN position.

53 to ON position. Test emitter B will illuminate.

Press reset button on pulse counter. The counts over a 100 sec. period will be recorded, and must be greater than 5 pulses per second (pps).

S3 to OFF position, test emitter will extinguish.

6.2. Channel A and Single Head

Reposition head to align channel A with test emitter B.

Switch on adaptor to position A.

S3 to ON position, test emitter 8 will illuminate.

Press reset button on pulse counter. The counts over a 100 sec. period will be recorded, and must be greater than 5 p.p.s.

S3 to OFF position, test emitter will extinguish.

S8 to position OUT.

7. EMITTER CHECK 320V

7.1. Channel A (Dual Head) and Single Head

Adaptor switch to EMITTER position.

\$7 to position 5.

D.V.M. shall read 320- 5V.

58 to position IN.

The emitter on channel A will illuminate, and the discharge shall occur across the narrowest gap of the electrades, for a period of not less than 30 secs.

S8 to position OUT.

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GRAVINER LIMITED, COLUBROOK, ENGLAND.	DATA SHEET No.	33.4
QUALITY CONTROL DATA SHEET	SHEET. No.	No. OF SHEETS
GUALITY CONTROL DATA STEET	10	

TITLE: DRAFT ACCEPTANCE REQUIREMENTS FOR 53521-012

AND 53522-011 HIGH TEMPERATURE U.V. DETECTORS PART &. GRAVING PROPHERD THEFTING PROCHIURS.

7.2. Channel B (Dual Head)

Adaptor switch to position B.

S8 to position IN.

The emitter on channel B will illuminate, and the discharge shall occur across the narrowest gap of the electrodes, for a period of not less than 30 secs.

SB to position OUT.

8. EMITTER CHECK 280V

8.1. Channel B (Dual Head)

S8 to position OUT.

S7 to position 6.

D.V.M. shall read 280V = 5V.

S8 to position IN.

The emitter on Channel B will illuminate. The discharge shall occur across the narrowest gap of the electrodes, for a period of not less than 30 secs.

58 to position OUT.

8.2. Channel A (Dual Head) and Single Head

Switch on Adaptor to position A.

Switch S8 to position IN.

The emitter on Channel A will illuminate. The discharge shall occur across the narrowest gap of the electrodes, for a period of not less than 30 secs.

S8 to position OUT.

SI to position OFF, LPI will extinguish.

9. MEGGER CHECK

Só to position 2.

Plug a 500V megger into sockets marked megger, ensure that the 'croc' clip on the yellow flylead is connected to the metal case of the head on test. The megger when energised should read mere then 20 megahns.

10. SOLAR

NOTE: Care should be taken not to subject personnel eyes to light emitted by the

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DATA LIMITED, COLNBROOK, ENGLAND. SHEET No... No. OF SHEETS SHEET, No. QUALITY CONTROL DATA SHEET DRAFT ACCEPTANCE REQUIREMENTS FOR 53521-012 TITLE: AND 53522-011 HIGH TEMPERATURE U.V. DETECTORS PART & GRAVIES PREFERENCE TESTING PROCESSING. 10. SOLAR (contd.) solar lamp. Slide gate on lamp to be closed before switching lamp on. 10.1. Channel A (Dual Head) and Single Head Só to position 1. S8 to position OUT. \$7 to position 1. Adapter switch to position A and position PHOTOCELL. Mount head to adapter on solar lamp, with channel A nearest source. Turn solar lamp on and allow to warm up for 5 minutes. SI to position ON, LPI illuminates. D.V.M. to read 320V - 5V. Place cover over head and filters. Open slide gate on lame. S8 to position IN. Press reest button on pulse counter. The counts over a 100 sec. period will be recorded, and must be less than -(See para. 5.6.). Clase slide gate on lamp. S8 to OUT. 10.2. Channel 8 (Dual Head) Adoptor switch to position B. Move head so that Channel B is nearest source window. Place cover over head and filters. Open slide gate on lamp. S8 to position IN. Press reset button on pulse counter. The counts over a 100 sec. period will be recorded, and must be less than -(See para. 5.6.). Close slide gate on lamp. S8 to OUT.

Disconnect head from fixture.

END OF TEST

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(DUALITY	CON	TROL	DATA	SHE	ET	811	EET. No.	12	No. OF SHEETS
TITLE:		3522-0	II HIGI	H TEM	PERATU	RE U.V	S 53521-	CTORS		
NOTE:	If the so before it					od of at	least 30	D minute	s must e	oliapee
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	DATA SHEET No.	a	2308
QUALITY CONTROL DATA SHEET	SHEET No.	1	No. OF SHEETS

TITLE:

ACCEPTANCE REQUIREMENTS FOR 53813-202 CREW WARNING UNIT PART A.

1. DEFINITION

Q.\$166 becames a master document for functional performance testing of Crow Warning Unit.

Performance values have been defined in compliance with "funnel" or "tiered telerances" philosophy and form the following entegeries.

- Type 1 Fectory or Production Acceptance Limits appropriate at normal ambient temperature conditions.
- Type 2 Receiving Inspection or Customer Acceptance Limits appropriate of named ambient temperature associations.
- Type 3 Quality or Functional Acceptance Limits appropriate at and between the declared extremes of appropriates.

In any report of test in two geographical areas there is expected to be some difference in test results. Differences within the stated occuracy of instrumentation and these due to acceptable variances based upon time dependency, transportation and test techniques are declared as acceptable. To most these alreamateness Type 1 limits used for Factory tests allow a smaller variation than there used for Type 2 limits by Receiving inspection and as Customer Acceptance. These tests are carried out at normal ambient temperature conditions.

Functional limits at extremes of operating conditions are determined and declared. From time to time quality qualit tests may be carried out and performance characteristics are measured for compilence with values of the appropriate which are measured at appropriate extreme conditions, particularly with respect to temperature. Type 3 limits enter for functional acceptance characteristics and allow a greater variation than Type 2 limits.

The current acceptance value applicable to the nature of the test is detailed in a schedule and is to be selected for use as appropriate. Any specified test where a single value remains in the test is applicable to Type 1, 2 and 3 tests.

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	QUA	LTY	CON	TROL	DATA	SHEE	. T	SH	OET No.	2	No. OF SHEETS
TITLE:	ACK	irta.	NCE RE	QUIRE		FOR 5	3813-2	22 CREW	WARN	ING I	JINIT
2.	FREG	MEN	CY OF	TEST							
	The f	iollon	ing tool	n shell	be certi	tuo bei	at a fee	drauch	approp ri	ete to	definition.
	Туре	1	All uni	w.							
	Туре	2		common i in use				receipt	" and su	pooqu	untily a
	Туро	3	These v	vill be	cerried	out as	oppropr	iete upo	m:		
			a)	initie	etion of	produc	etten.				
			b)	latro	duction	of a m	ojor me	dificatio	on.		
			c)	Case	otion of	produc	:Hen fo	r 6 mont	hs or mo	re.	
			d)		duction lards.	of nov	proces	nos whic	api waaa a	ffect	production
			•)	Cha	go of k	ey epe	refer.				
		•	os shell od the pr					•	reductie	n and	shall previously
	ln es	init o Lan	n, samp	ling she	di be e	s follow	A:				
	for n	•									sciected
3.	ACT	ON	REQUIR	£D							
					l result	. shadi i	DO 1000	rded age	inst the	sertel	number of each
		COA	trol un	lt.							
			Type 3 her of a						three pr	s agai	not the serial
	3.2.								the Dec	nign A	uthority.
	· ·	For	Type 3	tests co	ntrel u	nit that	fet la e				oli be exemined
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FITLE: ACCEPTAN	NCE REQUIREMENTS FOR 53813-202 PART A.	CREW WARNIN	G UNIT
be to	additional unit shall be taken for test aken to release the batch and to make is, test requirements, production tech apriote.	amendments to i	nepection require-
	RODUCTION ACCEPTANCE TESTS persont Required for Tests		
	0.5 A stabilised supply variable from	n lóv to 29v DC.	
2.	0 to 30v DC digital valt mater (DVN 1 magains.	with minimum in	nput resistance of
3.	0 - 0.2A DC ommeter.		
4.	Four 3K6 2% .5w resister.		
5.	500v DC insulation tester.		
6.	Ohm motor.		
4.2. Elec	trical Connections		
1.	Connect two of DC power supply via 6.	an anumeter to co	annector pin number
2.	Connect two of voltage to two of (C power supply.	
3.	Connect the -ve of DC power supply	to cannect pin n	umber 5.
4.	Connect a 3K6 resister between conn	ector pin number	9 and 5.
5.	Connect a 3K6 resister between conn	ector pin number	10 and 5.
6.	Cannect a 3K6 resister between cere	ector pin number	11 and 5.
7.	Connect a 3K6 resister between conf	ector pin number	12 and 5.

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G	AYME	Rum	TED, COL	NBROOK	ENGLAND.	DATA SHEET NO.	۵	5308
QL	IALITY	CON	TROL	DATA	SHEET	SHEET No.	4	No. OF SHEETS
TITLE:	CCEPTA	NCE I	REQUES		FOR 53813-	-202 CREW WARN	IING	UNIT
4.	3. Elec	etrical	Require	ments .				
	Not	e: The	limits	ae bja	n in the sele	adule of test ilmit	s, pan	s. 8.0.
	4.3	.1. <u>հ</u>	ndi cutor	Function	onal Chadle	•		
		S	at the [)C ###	ly to lév.			
	4.3	-	L ENG	FIRE" d A and-	rould show.	y via an ammeter The current draw Discompat number	n shou	id be between
·	4.3	.	UFIRE I	DET FAI	L" should sh mA and ——	y via an ammeter sw. The current 	drown	should be
	4.3	•	R ENG	FIRE" d	rould show,	y via an anumeter. The current draw isconnect pin mus naci.	n show	neewied ed bis
	4.3	-	R FIRE	LET FAI A and -	L" should sh	y via an ammeter ow. The current Discensest pin n atmost.	drawn	should be betwe
	4.3	.6.]	est Swi	tch Fund	ticasi Test			
		1 6	Depress ' On the D The cum Voltage	FAIL II .V.M. est dev	ND. TEST" a should be wi m should not	M. to connecter witch and held. thin V to a cacased N to a cacased	The vo	oltage indicated -V. please switch.
ICAUE	A	В	c	8				
wa								
COMPLED	Ps	Ps	P.	An				
		ī	1	1	1 1	1 1		1
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	ALTY						SHI	EET No.	5	No. OF SHEETS
TITLE:	CCEPTA	WCE RE	QUIRE		FOR 5		02 CREV	V WARN	ING I	UNIT
	4.3.	De D. no	pres "l V.M. i t exces	FAIL IN should b sd r	ND. TES be withing. Re	in'	tch and I V to to switc	V. The	oltoge e curr tage	wher il. indicated on ent drawn should to equal supply pin il.
	4,3.	De the abo	pres H D.V.: ould no	he "FIRI M show t excess Carres	E DET. uld be v	TEST" : within = mA. R	rwitch an V to lolowe th	V. he switch	Volt The	mber 10. lage indicated on current drawn plage to equal DVM from
	4.3.	De the she	press the D.V	he "FIRI M. she It exces	E DET 1 uld be v ud	EST" w within - mA. Re	witch on 	oV. no switch	Volta The Vo	mber 9. ige indicated on ' current drawn itage to equal DVM from
4.	.4. Set	the supp	dy to 2	the and	repeat	teets of	, 4	.3.2. 10	4.3.	9.
4.	.5. Con	neciten	i for too	its pare.	. 4.6.	teefs.				
	1)	Discon	neat the	9 +v9 ol	f DC pc	wer wp	aply from	n connec	tor pi	in number 6.
	2)	Disser	met the	• -w d	f the Di	C power	r wap ly	frem con	meck	or pin number 5.
	3)	Conne	n 11-0 +	⊶ of D	C power	w to asi	e Racker	pin numb	⊯ 5.	
	4)	Catana	st the -	→ of D	C power	n sepply	y to com	nactor pi	in nu	nber 6.
	5)	Connec	# *** 0	₩ D.V.	M. 10	tve of [• ••••••	w wpply.	•	
		Set DC						- , •		
4.	.6. Con Dep	neci-v	e of D. All INC	V.M. I	to comm	h, voin			should	d not exceed
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GRAYMER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No.	53.8
QUALITY CONTROL DATA SHEET	SHEET. No.	No. OF SHEETS

TITLE :

ACCEPTANCE REQUIREMENTS FOR 53813-202 CREW WARNING UNIT PART A.

- 4.6.2. Connect the of DVM to connector pin number 10.

 Depress "FIRE DET, TEST". Voltage on DVM should not exceed -----V. Disconnect the of DVM from pin 10.
- 4.6.3. Cannect the of DVM to cannector pin number 9.
 Depress "FIRE DET. TEST". Voltage on DVM should not exceed -----V. Discensest the of DVM from pin 9.
- 4.7. Connections for pure 4.8 tests
 - 1) Cannot alimnater between connecter pin number 5 and pin number 14.
- 4.8. Cantral Unit Reset Switch Tests
 - 4.8.1. Depress and hold "FAIL IND, TEST" switch. Resistance on alumenter should not exceed ----ahm. Release "FAIL IND, TEST" switch.
 - 4.8.2. Disconnect lead from pin 14 and connect to pin 7. Depress and hold "FIRE DET, TEST" and "FAIL IND, TEST" switches.

 Resistance on ahmmeter should not exceed ----ohm.

 Release "FIRE DET, TEST" and "FAIL IND, TEST" switches.
- 4.9. Connections for pare. 4.10. tests.
 - 1) Remove oil connections from connector.
 - 2) Link all connector pins together.

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C	WALIT	CON	TROL	DATA	SHEE	T	844	ET. No.	7	No. OF SHEETS
TITLE : A	CEPTAN	ICE REC	RUIREM	ENTS F	FOR 5381 RT A.	3-202	CREW V	WARN II	NG UN	NIT
4.	10. <u>Insul</u>	ation Te	tat							-
					ion tester ould not					tween all
5. <u>T</u>	/PE 2. C	USTON	ER REC	EIVIN	G TESTS					
Te	ets as Typ	pe I. P	ero. 4.1) . to 4	.4.					
N	ote: The	limits o	we give	n in th	o schody	le of te	et limit	s, para	8.	
6. <u>T</u>	PE 3. C	QUALIT'	YAND	FIELD	LIMITS					
N	ote: The	limits o	re give	n in th	e schedu	le of te	nt limit	s pero.	8.	
6.	1. Non	-Destruc	ctive Te	oh:						
	The	followin	ig lests :	shell be	e carried	œ∤.				
6.	2. Room	Tempe	rature T	osh.						
	Тура	1 tests	para. 4	. l. to	4.10. a	nd Type	l limi	n apply	•	
6.	3. <u>High</u>	Temper	oture To	ests +7	1°C					
	iong	erature	at +719	C for 3		_	·			. Maintain 29 v .
6.	4. <u>Low</u>	Temper	oture Te	oh -54	<u>MC</u>					
	-549		hrs. C		refrigera					perature at Justive
6.	5. Rope	naf room	temper	olure to	eets of po	wa. 6.1	2.			
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GRAVERER LIMITED, COLNEROOK, ENGLAND. DATA SHEET No. 053-8 SHEET.No. 8 No. OF SHEETS

TITLE:

ACCEPTANCE REQUIREMENTS FOR 53813-202 CREW WARNING UNIT PART A.

6.6. Destructive Tests

The following tests shall be carried out.

6.7. Room Temperature Tests

Type I tests para. 4.1. to 4.10. and Type I limits apply.

-6.8. High Temperature Tests +719C

The control unit shall be subjected to the high temperature test requirement of MIL-STD-810C, Method 501.1. Procedure 1 for a period of 48 hours. At the end of this time the functional tests of para. 4.3.2. to 4.3.5. should be carried out at 16v and 29v.

6.9. Low Temperature -54°C

The cantrol unit shall be subjected to the low temperature test requirements of MIL-STD-810C. Method 502.1. Procedure 1 for a period of 48 hours. At the end of this time the functional tests of para. 4.3.2. to 4.3.5, should be carried out at 16v and 29v.

7.0. Temperature Shock

The control unit shall meet the temperature shack requirements of MIL-STD-810C Method 503. Procedure 1, and shall be uneffected by rapid transfer between the following temperatures:

After this test the control unit should not have sustained any mechanical damage and should meet the requirements of para, 4.1. to 4.10, and room temperature limits at 16v and 29v.

7.1. Vibration

The control unit shall meet the vibration requirements of MIL-STD-810C, Method 514.2. Precedure 1A. The unit shall be subjected to random vibration

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GRAVINER LIMITED, COLMBAOOK, ENGLAND.	SHEET No.	53 <i>0</i> 8
QUALITY CONTROL DATA SHEET	SHEET. No.	No. OF SHEETS

TITLE:

ACCEPTANCE REQUIREMENTS FOR 53813-202 CREW WARNING UNIT PART A.

7.1.cont.

in each of 3 mutually perpendicular axes. The test shall be over the frequency range of 15 - 2000 Hz. at the vibration levels and test times detailed in Fig. 514.2-11A and 514.2-2A of MIL-STD-810C.

The unit shall function as required by tests of paras. 4.3.2. to 4.3.5. during and 4.1. to 4.10. after test.

8. Schedule of Tests

PARA.		TYPE 1	TYPE 2	TYPE 3
4.3.2.) 4.3.3.)				
4.3.4.	160	62 mA and 81 mA	59 mA and 84 mA	59 mA and 87 mA
	29√	93 mA and 112 mA	90 mA and 115 mA	90 mA and 118 mA
4.3.6.		1.3v to 2.0	1.0v to 2.2	N/A
4.3.7.	164	9 mA	10 mA	N/A
4.3.8.	29√	1.3v to 2.0	1.0v to 2.2	N/A
4.3.9.		16 mA	17 mA	N/A
4.5.0.				
4.6.1.		-0.3√	-0.35v	N/A
4.6.2.		-0.50	-5.50	1
4.6.3.				
4.8.1.		0.025 ohm	0.025 ahm	0.025 ahm
4.8.2.		0.050 ohm	0.05u ahm	0.050 ohm
4.8.3.		0.025 ehm	0.025 ahm	0.025 ahm
4.10.		20 magahms	20 megahas	20 megahms

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- ,					ATA S		SHEE	T. No.	10	No. OF SHRETS
TITLE :	ACC						2 CREW WA		-	
1.	EQU	IPMEN	IT REQU	IRED						
	DC ().V.M	١.							
	A.V.	.O. M	8 lebal							
	0.54	0-30	v Variabl	• DC m	pply.					•
	Ohm	moter								
	Test	Equipa	ment	G.I		Adoptor	F16.2.	-		
2.	<u>CO1</u>	INECT	IONS A	ND SET	INGS					
	2.1.	SW	land SM	/2 to OF	F.					
	2.2.	sw	3 to POS	1						
	2.3.	Con	mest DV	M to DV	/M Termi	nais.				
	2.4.	Con	unact AV	OhAV	/O Ternal	nals				
	2.5.	Set	AVO O	N 0-100	mA Sca	e Œ.				
	2.6.	Ca	nnect Por	ver Supp	dy to 16-	29v Term	inals.			
	2.7.	Set	Supply 1	o lóv						
	2.8.	Tur	n Supply	OFF.						
	2.9.	Cas	nnest Un	it to Tee	t Set.					
3.	TEST	PROC	EDURE							
	3.1.	Tur	n Power	Supply	Power O	N, LED N	b Light.			
	3.2.			•••		to Light	•			
	3.3.	Rec	od Curren	1m	A. Paro	. 4.3.2.				
	3.4.	Set	SW2 to	2, L.EN	G FIRE	O EXTIN	GUISHER,	Left "	FIRE C	ET FAIL" to L
	3.5.	Rec	d Curren	tm	A, Paro	. 4.3.3.				
	3.6.	Set	SW2 to	3, Left '	FIRE DE	T FAIL" to	o extinguish	, REN	NG FI	RE to Light.
	3.7.	Rec	ed Currer)tm	A. Para	. 4.3.4.				
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GRAVINER LIMITED, COLNEROOK, ENGLAND.

DATA SHEET No.

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QUALITY CONTROL DATA SHEET

SHEET No.

No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR 53813-202 CREW WARNING UNIT PART B. PREFERRED GRAVINER TEST PROCEDURE WITH TYPE 1 LIMITS

3. TEST PROCEDURE (cantal.)

- 3.8. Set SW2 to 4, 'R.ENG FIRE' To Extinguish, "R.FIRE DET FAIL' to light.
- 3.9. Read current ----mA, Para. 4.3.5.
- 3.10. Set SW2 to OFF, 'R .FIRE DET FAIL' to extinguish.
- 3.11. Set SW1 to 1. Set Avo to 0-100mA range.
- 3.12. Depress and hold "FAIL IND TEST".
- 3.13. Read DVM ---- Velts and AVO ----mA, Page. 4.3.6.
- 3.14. Release "Fell IND TEST".
- 3.15. Set SW1 to 2.
- 3.16. Depress and hold 'FAIL IND TEST'.
- 3.17. Road DVM ---- Volts and AVO ---- mA, Pare. 4.3.7.
- 3.18. Roloss "FAIL IND TEST".
- 3.19. Set SW1 to 3.
- 3.20. Degrees and held "FIRE DET TEST".
- 3.21. Read DVM ----- Volta and AVO ----- mA, Para. 4.3.8.
- 3.22. Release "FIRE DET TEST".
- 3.23. Set SW1 to 4.
- 3.24. Depress and hold "FIRE DET TEST".
- 3.25. Read DVM ----- Yalts and AVO ---- mA, Pare. 4.3.9.
- 3.26. Sat SWI to OFF.
- 3.27. Set Power Supply to 29v. Set Avo to 0-1A range.
- 3.28. Repeat Pera. 3.2. to 3.26. Inclusive.
- 3.29. Set SW3 to 2.
- 3.30. Set SW1 to 1.
- 3.31. Depress and hold "FAIL IND TEST".

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						SHEET		SHEET, No.	12	No. OF SHEETS
TITLE:								W WARNI WITH TYP		IIT
3.	TEST PR	OCEDI	JRE (co	entd.)						
	3.32.	Read D	VM	Va	dn. f	ara 4.6.				
	3.33.	3. Release "FAIL IND TEST".								
	3.34.	3.34. Set SW1 to 2.								
	3.35.	Depres	and h	old "I	FAIL II	ND TEST"	•			
	3.36.	Read D	VM	Vo	its. f	lore . 4.6.	1.		•	
	3.37.	Release	"FAI	. IND	TEST"	· ·				
	3. 38 .	Set SW	1 to 3							
	3. 39 .	Depres	and h	old "I	FIRE D	ET TEST".				
						ero . 4.6.	2.			
	3.41. Release "FIRE DET TEST".									
	3.42.									
1		•				ET TEST".				
i						Para. 4.6.	3.			
	3.45.				TEST"					
	3.46.									
	3.47.									
	3.48.			•		_				
·	3,49.						_		• -	
			-		-	•	-	d pin numb	er 14.	
	_		_	-		ET TEST".				
						. Paro. 4	. 			
	3.53.									
	3.54.					•				pin number 7.
	3.55.	Depres	ond t	told "	FIRE U	E1 1521-	ond "FAI	L IND TES	1".	
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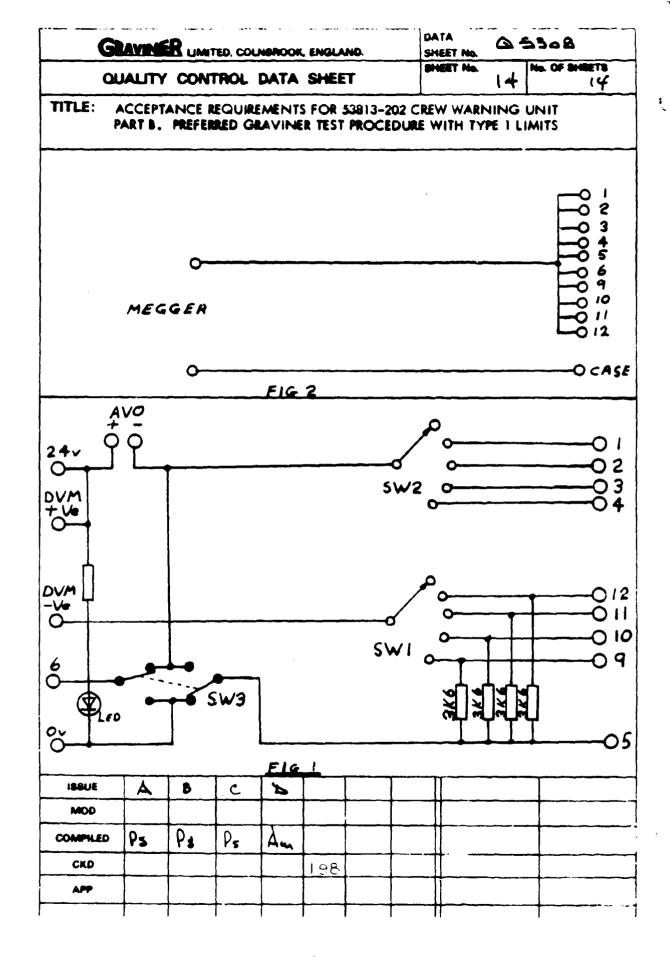
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			CON						BET. No.	13	No. OF SHEETS
TITLE	ACCE							CREW N		4G U	
3.	TEST F	ROC	EDURE (contd.)							
	3.56.	Rea	d ohne) ter	- ohm.	Para	4.8. 2.				
								TEST"			
										et to s	oin number 14.
			rees and			•			y	- •	
		•	d chan								
	3.61.	Rek	oces "F/	ML 840	1EST	٠.					
	3.62.	Die	connect	ohanne	er from	n unit.					
	3.63.	Con	mect un	it to Ac	laptar -						
	3.64.	Con	inect Mi	egger bi	stwaan	case of	i unit c	nd lead	af adap	ter.	
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GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No.	5509
	SHEET. No.	No. OF SHEETS

TITLE:

ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

(i) Definition

Q53-9 becomes a master document for function performance testing of Control Unit 53813-203.

Performance values have been defined in compliance with "funnel or tiered tolerances" philosophy and form the following categories.

- Type 1 Factory or Production Acceptance Limits oppropriate at normal ambient temperature conditions.
- Type 2 Receiving Inspection or Customer Acceptance Limits appropriate at normal ambient temperature conditions.
- Type 3 Quality or Functional Acceptance Limits appropriate at and between the declared extremes of operating temperatures.

In any repeat of test in two geographical areas there is expected to be same difference in test results. Differences within the state diaccuracy of instrumentation and those due to acceptable variances based upon time dependency, transportation and test techniques are declared at acceptable. To meet these circumstances Type 1 limits used for Factory tests allow a smaller variation than those used for Type 2 limits by Receiving Inspection and as Customer Acceptance. These tests are carried out at normal ambient temperature canditions.

Functional limits at extremes of operating conditions are determined and declared. From time to time quality audit tests may be carried out and performance characteristics are measured for compliance with values of the approval sample which are measured at appropriate extreme conditions, particularly with respect to temperature. Type 3 limits cater for functional acceptance characteristics and allow a greater variation than Type 2 limits.

The correct acceptable value applicable to the nature of the test is detailed in a schedule and is to be selected for use as appropriate. Any test where a single value remains in the text is applicable to Type 1, 2 and 3 tests.

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	GBAY	MER LIMITED, COLNEROOK, ENGLAND.	DATA SHEET No. Q 5309	
	QUAL	ITY CONTROL DATA SHEET	SHEET, No. 2 No. OF SHEET	18
TITLE	ACC	EPTANCE REQUIREMENTS FOR U.V.A. 3-203 (SYSTEM A)	F.D.S. CONTROL UNIT	
(ii)	Frequenc	cy of Test		
	The follo	owing tests shall be carried out at a frequ	vency appropriate to definition.	
•	Type 1	All units.		
	Type 2	It is recommended that all units 'on re defined in users procedures and schedu		
	Type 3	These will be astribed out as appropria	te upen:-	
		Initiation of production. Introduction of a major modification. Committee mont Introduction of new processes which m Change of key operator.		
(ili)	Action R	beniupe		
	iii(o)	For Type 1 tests all results shall be re- control unit.	carded against Serial No. of each	
		For Type 3 tests an abridged test report Serial No. of each control unit is reis		•
	ili(b)	For Type 1 tests any failures shall be a	reported to the Design Authority.	
		For Type 3 tests, any Central Unit that shall be examined to locate the partic causing the malfunction.		
		The defective sub-assembly shall be re sub-assemblies, and repeat testing car	·	
		Subject to satisfactory results on both	replacement sub-assemblies,	

the batch of units can be released.

A follure during re-test on either sub-assembly constitutes a foilure of the whole batch, and rectification/design modification is required before the batch can be released.

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probes.

Pulse select unit as per Fig. 11 (calibrated as per Appendix 2)

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	GRAYNER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No	5309
	QUALITY CONTROL DATA SHEET	SHEET. No.	No. OF SHEETS
TITLE:	ACCEPTANCE REQUIREMENTS FOR U.V.A 53813-203 (SYSTEM A)	.F.D.S. CONTROL	UNIT

2. CONNECTIONS

Check that all supplies are set to OFF. Connect control unit to supplies and test equipment as per Fig. 4.

3. INITIAL SETTINGS

- 3.1. \$1A, \$2A, \$3 and \$4 a n Meter and Supply Switing Unit to OFF.

 All 4 meters switch on Meter and Supply Swithing Unit to A.
- 3.2. Rotary switch on GSE control unit to position 4.
- 3.3. GSE made switch to IN.
- 3.4. Date switch to A.
- 3.5. Computer cord boud rate settings to 30 characters/sec.
- 3.6. All head simulation unit, F1 (fire and FA fault) switches all to eff.
- 3.7. M1 and M2 set to 1 amp range AC.
- 3.8. M3 set to 1 Amp range DC.
- 3.9. M4 set to 10 mA range DC.
- 3.10. Using DVM set to 200V AC range switch on AC supply and set it to 124V 420 Hz (= 0.5V).
- 3.11. Using DVM set to 50V DC switch on V1 and set it to 29V (+0.1V).
- 3.12. Using DVM set to 10V DC switch on V_2 and set it to 4V (-0.1V).
- 3.13. Using DVM set to 10V DC range, disconnect positive lead to V3 supply. Switch on V3, set it to 5.6V (-0.2V). Switch off V3 and reconnect positive lead.
- 3.14. Head select switch an Pulse Simulation unit to OFF.

4. TEST PROCEDURE

Notes: 1) Meter M4 should be observed at each test and unless stated otherwise should read zero current.

2) Limits of all tests are contained in Appendix 1.

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Q	UALITY (CONTROL DATA	A SHEET	SHEET, No.	5 No. OF SHEETS
		ICE REQUIREMENT (SYSTEM A)	TS FOR U.V.A	A.F.D.S. CONTRO	
4. TES	T PROCEDI	URE (contd.)			
4.1	. Earthin	ng Connections			
			-	ce bridge, check re blug, resistance to i	esistance be less thanohms
4.2	. Prelimi	inary Check Out (I	High Supply Vo	oltoges)	
	4.2.1.			forms to CCU as per read less than	
		Switch S3 to on	. M3 should re	eod less than	mA,
		CWU left hand	'FIRE DETECT	FAIL' lamp to illum	ninote.
	4.2.2	within I second	l of each other.	s, SIA and S2A sho . Observe that GS upport Control Unit	SE 1 LEDS on
		MI to indicate	less than	mA.	
		M2 to indicate			
		M3 to indicate		mA .	
		M4 to indicate	zero mA .		
4.3	Prelim	inary Check Out	,		
	4.3.1	observe that GS	SE 1 LEDS on G 3 per second.	OUT, depress and re GSECU flash alterna GSE 2 LEDS should seconds.	ately at a rate of
				lamps i.e. 'L ENG oth extinguished.	.FIRE' and 'FIRE
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		CONTROL	SHEET. No.	No. OF SHEETS				
TITLE:		ANCE REQU 03 (SYSTEA	UIREMENTS FOR U.V.A					
	4.3.2	to indic	'FIRE DETECT TEST' pur ate within approximatel	y one second.	·			
			'FIRE DETECT TEST' pur gulsh within <mark>approximat</mark>		J, LENGTIKE IOMP			
		•	'FAIL IND, TEST' push' 'FAIL' lamp to show.	button on CWU,	left hand 'FIRE			
•			'FAI IND. TEST' push 'FAIL' lamp to extinguis		left hand 'FIRE			
4.4.	Suppl	y Currents -	Running Made					
	Note:		dicate less than		share. Observe			
	M3 to	indicate le	ms than mA.					
	M4 to	indicate z	ero.					
4.5.	Suppl	y Currents	- Fire Mode					
	•	es and hold re meter rea	CWU Fire Test button, adings.	when 'L ENG FI	RE' lamps show,			
	M1 or	nd M2 shoul	ld read less than	mA .				
	M3 sh	l boen bluoi	ess than mA.					
		sould read a						
			s test button.					
4.6	Prolin	ninary Chec	k Out (Low Supply Volt	rages)				
		•	/S2A, S3 and S4 to OFF vitch on GSECU to IN.	•				
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DATA SHEET No....

Q 5309

QUALITY CONTROL DATA SHEET

SHEET, No.

No. OF SHEETS

TITLE :

1

ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.6. Preliminary Check Out (Low Supply Voltages) (contd.)

Repeat 4.2 to 4.5. inclusive with power supply settings as follows:-

Using DVM set

AC supply to 102 volts 380 Hz (* 0.5V)

V1 supply to 16 volts DC (+0.2V)

V2 supply to 3 volts DC (* 0.1V)

Repeat 4.2 to 4.6 inclusively, then set S1A/S2A, S3 and S4 to OFF.

4.7. Regulation Operation

Note: All DC voltages are measured with respect to pin 32 of manitoring points.

4.7.1. Settings (Low Supply)

Using DVM set

V1 to 28 volts DC (+ 0.2V)

Set V2 to 3.6 valts DC (+0.1V)

Set GSE made switch on GSECU to IN.

- 4.7.2. Set switches SIA/S2A, S3 and S4 to ON.
- 4.7.3. Regulation at low supply (5.6V rail) side 1.

With DVM set at 10V range DC, check voltage at pin 12 of monitoring points. Voltage to be between ----- volts minimum and ----- volts maximum.

4.7.4. Regulation at low supply (5.6V rail) side 2.

Repeat 4.7.3, with DVM connected to pin 18 of monitoring point.

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	AUTY (·			EET. No.		No. OF SHEETS		
TITLE: A	CCEPTAN 3813-203	NCE	REQUIR	EMEN			.F.D.S		ROL UN		
	4.7.5	Re	aulatia	n at lo	w suppl	v (head	supply)	side 1.			
			_		• •	•		ESE TER/	MINALS	•	
		mo		g point	, volta	ge to be	betwee	oltage a m	•	of ts minimum	
4.7.6. Regulation at low supply (head supply) side 2.											
	Repeat 4.7.5. with DVM connected to pin 39 of monitoring										
		Se	t switch	100 SIA	/S2A,	S3 and	54 to C	FF.			
	4.7.7	<u>Se</u>	ttings (High Si	уррі у)						
			ing DV 7.6 inc			ly to 12	R4V 420	Hz. Rej	est 4.7	.2. to	
4.8.	Timing	Test	<u>.</u>								
	4.8.1.	<u>Se</u>	ttings f	or Powe	or Up T	ime Del	oy				
		W	ith Swit	ches S	IA/S2A	, S3 an	d S4 to	OFF set			
		A	Supply	to 401	Hz 11	5V (± 0	.5∨).				
		to		m trigg	ering to	positiv	•	cm, cha channel		and 2 amps. stored	
		Se	t chann	ellon	ed 2 to	DC mad	.				
		Se	t storag	e mode	to RO	LL.					
			t GSE n								
		Sw	itcho n	oscillo	ecope d	and odju	at it suc	h that c	honnel	l trace is at	
		mic	1 1C/06N	and ci		215 2 C	m obove	bottom	of scree	n.	
								,			
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	SRAYMER LIMITED, COLNERDOK, ENGLAND.	DATA SHEET No	5309
	QUALITY CONTROL DATA SHEET	SHEET. No.	No. OF SHEETS
TITLE:	ACCEPTANCE REQUIREMENTS FOR U.V.A		UNIT

4.8.2. Connections for Power Up Time Delay

Connect CH1 to terminal block maniforing point 23.

Connect CH2 probe to terminal block maniforing point 12.

All probe returns are connected to pun 32 of manitoring point.

- 4.8.3. Power Up Time Delay (Side 1)
 - 4.8.3.1. With oscilloscope trigger armed switch on system power in the order S3 and S4, S1A/S2A observe waveform as per Fig. 5.

Note: If oscilloscope does not trigger, adjust trigger level in conjunction with setting SIA, S2A to off, re-arming trigger and setting SIA/SIB back to ON.

Measure time delay between rising edge of channel 1 and 2 as shown in Fig. 5.
Set SIA/S2A, S3 and S4 to OFF.

4.8.3.2. Power up Time Delay (Side 2)

Repeat 4.8.3.1. but with Channel 1 probe connected to terminal block manitoring point 41 and Channel 2 probe connected to manitoring point 18.

Remove callloscope probes from manitoring point.

4.8.4. Settings for Time Share Timing

Switch an timer counter.

Set GSE made switch to OUT.

Set timer for positive edge start, positive edge stop such that 500 mS can be measured.

4.8.5. Connections for Time Share Timing

Connect timer probe to monitoring point pin 23.

Probe return connected to monitoring point pin 32.

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		-	ONTROL					EET. No.	10	No. OF SHEETS
			REQUIRE	MENTS	FORU	J.V.A.	F.D.S.			ıt
	4.8	.6.	Side 1 Tir	ne She	•					
			4.8.6.1.	Set S	1A/S2A	, S3 ar	nd S4 to	ON.		
				System	n to fu	nction c	m per 4.	3.1.		
			4.8.6.2.					ne to be maximum		n 10 61.
			4.8.6.3.		to be -					imer. secs.
	4.8	.7.	Side 2 Tim	ne Sha	•					
			Repeat 4.	8.6. w	ith tim	er prob	onne	ted to m	onitori	ng point 41.
	4.8	.8.	Connection	one and	setting	s for Se	if Test	imer		
			Connect to Select time timer range	ur for	positive	edge :	start, po	citive ed	ge stop	, Select
	4.8	.9.	Side 1 Sel	f Test	Timing	(Period	չ			•
			Observe p							· 10C5 .
	4.8	.10.	Side 1 Sel	f Test	Timing	(Durati	on)			
			Reselect tobserve pominimum s	riod o	f timer.	Time	to be be	tween		
	4.8	.11.	Side 2 Sel	f Test	Timing					
			Repeat 4.1			0. but	with tim	er probe	connec	ited to
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QU	ALITY C	ONTROL DATA SHEET	SHEET, No.	No. OF SHEETS
		CE REQUIREMENTS FOR U.V.A. SYSTEM A)	.F.D.S. CONT	ROL UNIT
	4.8.11.	Side 2 Self Test Timing (contd.))	
		Remove timer probe from monito	oring point.	
4.9.	Ground	Support Voltage Lines		
	Note:	All DC voltages are manitored v	with respect to p	pin 32 of .
	4.9.1.	Settings		
		With power on from previous ter Depress and release reset button Observe that GSE1 LEDS on sid	on GSECU.	
	4.9.2.	System Definition Connection		
		With DVM set on 10V DC range monitoring points, voltage to be and		
	4.9.3.	Battery Monitoring Point		
		With DVM set to 10V range che point, voltage to be between -		
	4.9.4.	115V Feeds to GSE (Side 1)		
		BEWARE OF HIGH VOLTAGE	ON'THESE TERA	MINALS.
		Set DVM to 200V AC range and of manitoring point.	d connect probe	s to pins 10 and 11

Observe DVM reading between ----- volts maximum and ----- volts minimum. Set S2A to OFF and observe that DVM voltage does not change.
Return S2A to ON.

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TITLE	A			E REQUIR		TS FOR	U.V.A	.F.D.S	CONT	ROL U	NIT
		4.9	.5.	115V Fee	ds to C	SE (Sid	• 2)				
				BEWARE	OF HIC	3H VOI	TAGE	ON THE	SE TERA	AINAL:	S
				Set DVM of monito					•	•	ns 19 and 20
					o Off	and obs	mexim	um and		- volt	oltage to be minimum. ot change.
	4.10	. Che	ck Pa	oint Monit	oring					•	•
		4.1	0.1.	Settings o	and Co	nnection	<u>w</u> .				
				Set GSE (Depress a Set DVM Connect (manitarin	nd relate to 50 v	volt ran	ot switc	h on GS	ECU.	to pin :	32 of
		4.1	0.2.	Check Po	int 1						
				DVM rec	ding t	o be zer	ъ.				
				Depress 'I lamp to it minimum Release 'I	ndicate and ;	, DVM	reading	j to be b naximum	neewteen .		
		4.10	0.3.	Check Po	int 2						
				Repeat 4.			/M posi	tive con	nected	to pin i	29 of
		4.10	0,4.	Check Po	int 3						
				Connect I DVM read		•		itoring	points.		
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TITLE :

ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.10.4. Check Paint 3 (contd.)

Depress 'FAIL IND. TEST' push button, left 'FIRE DETECT FAIL' indication to show.

Observe DVM reading, voltage to be between ------ volts minimum and ----- volts maximum.

1.5. Check Point 4

Repeat 4.10.4. with DVM connected to pire 36 of monitoring point.

4.11. Ground Support Controlled Tests

4.11.1, RAM Test and Reset

Set GSE Mode switch on GSECU to IN.

Depress and release reset switch on GSECU.

Observe that side 1 and side 2 GSE1 LEDS on GSECU light.

4.11.2. Common Logic Test (Functional)

Select position 4 on rotary switch, depress and release reset button. Observe that GSE1 and 2 LEDS on GSECU flash on and off in the following sequence:

GSE 2 side 1 (ON-OFF), GSE1 side 1 (ON), GSE2 side 1 (ON). GSE2 side 2 (ON-OFF), GSE1 side 2 (ON), GSE2 side 2 (ON).

Repeat depression and release of reset button, observe that 'L ENG.FIRE' and left hand 'FIRE DETECT FAIL' lamps do not flash on during the period that GSE LEDS are active.

Set S1A/S2A, S3 and S4 to OFF.

4.11.3. Common Logic Test (Timing)

4.11.3.1. Connections and Settings

Set oscilloscope channels 1 and 2 amps to 0.2V/cm.

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	ACCEP1 53813-2			-	rs for	U.V.A	.F.D.S	. CONT	ROL L	INIT
		4.	11.3.1	. <u>Conn</u>	ections	and Se	ttings (d	contd.)		
				Set tr	igger h	CHI (positive	edge).		
				Set d	isplay n	node to	ROLL.			
				Set ti	me ba	10 0.	1 2004/0	≥m .		
				Set "	stored"	trigger	point to	trace	•	
				Conn	ect che	probe to	pin 23	of mon	itoring point.	
				Conn	ect cho	nnel 2	probe to	pin 3 o	f monit	toring point.
				Conn	ect prol	be retu	m lines	to pin 33	2 of ma	onitoring point.
		٠ 4.	11.3.2	. <u>Side</u>	l Timin	g of Co	mmon L	ogic Tes	<u>.</u>	
				Depre Arm o	ms and	hold re cope tri		on on G		button 2
		•		Wave	form to	be as i	Fig. 6.			
					njunctio	on with		ions of C		djust trigger level reset switch and
							of then			
		4.	11.3.3	. Side	2 Timin	g of Co	ommon L	ogic Ter	<u>ut</u>	
				Conn	oct cha	nnel 1	probe to	pin 41	of man	itoring point.
							•	•		toring point.
					or 4. i l		•	•		•
		4	11.3.4	. Inter	Channe	l Timin	a (Casa	ections)		
		**	- • • • • • •						•	
				Conne	ect chai	nnel 1	probe to	pin 23 d	of moni	itoring point.
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TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

- 4.11.3.4 Interchannel Timing (Connections) (Contd.)

 Connect channel 2 probe to pin 41 of maniforing point.

 Set time base to 0.5 secs/cm. Set'stored trigger point to 1 scale.
- 4.11.3.5 Interchannel Timing
 Set \$1A/\$2A, \$3 and \$4 to ON. Arm oscilloscope trigger.
 Depress and hold reset button on GSECU for 5 seconds.
 Release reset button on GSECU.
 Waveform to be as Fig.7. take measurement t.
 Remove oscilloscope probes.
- 4.11.4. Background Programme Test
 Select position 5 on GSECU rotary switch.
 Depress and release reset button.
 After 5 seconds no LEDS to show on GSECU.
- 4.11.5. Idle Programme Test.

 Select position © on GSECU rotary switch.

 Depress and release reset button.

 Observe that side 1 and side 2 GSE1 and 2 LEDS on GSECU show.
- 4.11.6. Data Retention Test.

 Set 54 to OFF. Select position 2 on GSECU rotary switch.

 Depress and release reset button.

 Observe that side 1 and side 2 GSE1 LEDS on GSECU light.

 Select position 3 on GSECU rotary switch, depress and release reset button.

Observe that side 1 and side 2 GSE1 and GSE2 LEDS on GSECU light. Resoluct position 2 on GSECU ratary switch, depress and release reset button.

Observe that Side 1 & 2 and GSEL LED's on GSECU light. Set S1A/S2A and S3 to OFF. Wait 30 seconds. Select position 3 on GSECU rotary switch. Set S1A/S2A and S3 to ON.
Observe that only side 1 and 2 GSE 1 LEDS on GSECU Light.

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	4.11	.6. <u>De</u>	ota Rete	ntion 1	est (co	ntd.)				
			melect ; it S4 to		2 on (SSECU	rotary s	witch.		
		QF	id side 2	GSE1	LEDS o	on GSE	CU light			that only side 1
		Se		mA mo S2A and	ximum. d 53 to	ON. (•			d less than
	4.11	.7. <u>D</u>	no Reac	out Te	<u>st</u>					
		4.	.11.7.1	. Side	Test					
							y to cor	nputer ca rinter.	rd).	
				Selec	t positi	an 2 an	GSECL	l rotary s	witch.	
				Depre	es and	re lease	reset sw	ritch on (SSECU	ı .
				Obee	ve that	side 1	and side	2 GSE1	LEDS	on GSECU light.
				Depre	es and		et switc	I rotary si th on GSI		
				Obser	ve that	printer	prints		٠.	
				Relea	ee recel	switch	on GSE	CU.		
				Printe	r shoul	d print	as Fig.	8.		
				When on G	•	stops o		that GSE	LEDS	(side 1 and 2)
		4.	11.7.2	. Side	2 Test					
				Repe	it 4.11	.7.1. N	est but v	with GSE	CU do	a switch set to B
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QUALITY CONTROL DATA SHEET

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TITLE:

ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.12. System Functional Tests

All fire and fault indications refer to 'L ENG.FIRE' and left hand 'FIRE DETECT FAIL' lamps on CWU.

Note: These tests are carried out using the head simulation unit referred to as HSIMU.

All references to side 1 fault and fire switches refer to System A side 1. System B fault and fire switches are not used.

4.12.1. Initialise for Functional Tests

With system still powered from previous tests, select position ó on rotary switch of GSECU.

Set GSE made switch to OUT.

Depress and release reset switch on GSECU. Observe that system functions as per 4.3.1.

4.12.2. Check for No Faulty Head Drive Circuits

Set all side I fire switches to ON. CWU fire lamp should remain off.

Set all side 1 fire switches to OFF. Set all side 2 fire switches to on. CWU fire lamp should remain OFF.

Set all side 2 fire switches to OFF.

4.12.3. 'ANDED' Head Operation

Set heads 5, 6 and 7 fault switches, sides 1 and 2 on HSIMU to ON. These to remain on for all subsequent functional tests of para. 4.12.

Note: Switch positions 0 - OFF 1 -ON.

Carry out ANDED TESTS according to sequence as follows, and observe CWU fire lamp status as shown.

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	4.12.3	. <u>'Al</u>	NDEI	D, H	eod	Operati	on (cor	ntd.)			
		HE.		SIDE		TCHES	HE	AD			2 WITCHES	CV FIR	/U ·
		8	4 3	2	1		8	4	. 3	2	1		
	1)	0 0	0 0 0	0 0 0	1 1 0		0	00	00000		1	())
	2)	0	0 0	1 0 0	0		0	0	0	0 1 1 0	0)
	3)		1 0 0	į					0 1 1 0				1
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TITLE :

ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.12.3. (Cont.)

	HE	AD		E 1 SW	ITCI	1ES	HE	AD	CWU S FIRE LAMP			
	8	4	3	2	1		8	4	3	2	1	
12)					1				-			0
13)			_								1	0
14)					1			1				0
15)		1									1	0
16)					1		1					0
17)	1										1	0
18)			1					1				U
19)		1							1			0
20)			1				1					0
21)	1								1			0
22)	0	0	0	0	0		0	0	0	0	0	0

Nate: All unmarked positions are assumed to be '0'

4.12.4. 'ORED' Head Operation Side 1

4.12.4.1. Set all side 2 head fault switches to ON.

Depress and release GSECU reset switch and observe that CWU fault indication does not light after the first occurrence of GSE2 (side 1 and 2) LEDS flashing on GSECU.

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TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.12.4.2. Set side 1 head 1 fireswitch to ON.

Fire indication on CWU to show.

Set side I head I fire switch to OFF.

Fire indication on CWU to extinguish.

- 4.12.4.3. Repeat 4.12.2.2. for heads 2, 3, 4 and 8.
- 4.12.4.4. Return side 2 fault switches 1, 2, 3, 4 and 8 to OFF.
- 4.12.5. 'ORED' Head Operation Side 2
 - 4.12.5.1. Set all side I fault switches to ON.

Depress and release GSECU reset switch, observe that CWU fault indication does not light after the first occurrence of GSE2 (side 1 and 2) LEDS flashing on GSECU.

4.12.5.2. Set side 2 head 1 fire switch to CN.

Fire indication on CWU to show.

Set side 2 head 1 fire switch to OFF.

Fire indication on CWU to extinguish.

- 4.12.5.3. Repeat 4.12.5.2. for heads 2, 3, 4 and 3.
- 4.12.5.4. Return side 1 fault switches 1, 2, 3, 4 and 8 to OFF.

4.12.6. Failed Heads

Set side 1 and side 2 heads 1, 3 and 4 fault switches on HSIMU to ON.

Observe that left hand 'FIRE DETECT FAIL' lamp does not light at next occurrence of GSE1 (side 1 and 2) LEDS fleshing an GSECU.

Set side 1 and 2 heads 1, 3 and 4 fault switches on HSIMU to OFF.

Set side 1 & 2 heads 2 & 8 fault switches on HSIMU to ON.

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ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT

4.12.6. Failed Heads (contd.)

Observe that left hand 'FIRE DETECT FAIL' lamp does not light at next occurrence of GSE2 (side 1 and side 2). LEDS flashing on GSECU.

4.12.7.

53813-203 (SYSTEM A)

TITLE :

4.12.7.1. Heads 1 and 2 adjacency Set

Set all side 1 and 2 fire and fault switches to OFF.

4.12.7.2. Set GSE made switch on GSECU to IN.

Depress and release reset button.

Left hand 'FIRE DETECT FAIL' lamp to be OFF.

Observe that side 1 and side 2 GSE1 LEDS on GSECU are lit.

Set heed 1 and 2 fault switches an side 1 and side 2 to ON.

Set GSE made switch on GSECU to OUT.

Depress and release reset button.

Left hand CWU 'FIRE DETECT FAIL' lamp should light immediately after the first occurrence of GSE2 (side 1 and 2) LEDS flashing on GSECU.

Set head 1 and 2 fault switches on side 1 and side 2 to OFF.

After the occurrence of the next flashing sequence of GSE 2 LEDS (occurring approximately once every 15 seconds) observe that left hand 'FIRE DETECT FAIL' lamp does not extinguish.

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		•	4.12.7.	3. Hea	ds 2 an	d 3 Ad	acency	Set		
				Rep	eat 4. l	2.7.2.	using h	eads 2 ans	d 3 foo	ult switches.
		•	4.12.7.	4. <u>Hea</u>	ds 4 on	d 8 Ad	acency			
				Rep	eat 4, 1	2.7.2.	using h	ead 4 and	8 fau	It switches.
		•	4.12.7.	swif Obe ligh	ich. Jerve th it.	at GSE	1 LEDS	on side 1	and si	release reset de 2 of GSECU satinguished.
	4.1	2.8.	Sensitiv	ity and	Short	Circuit	Head O	peration		
		•	4.12.8.	1 . <u>Set</u>	Up for	Side 1	Heads			
				Set	all side	1 foul	I switch	es to OFF	•	
								es to ON		
				Set	side 1	and 2 fl	re switc	hes to OF	F.	
							*		•	U) to side 1A.
								on PSU to		1.
								on PSU to		
								SSECU to		
				•				switch on		
				0	erve th	ot syste	m functi	ions as pe	r 4.3.	1.
			4.12.8.	2. Fire	Set (H	e od 1,	<u> 3ide 1)</u>			
				Not			conds at		tch po	sition before
				Set	PULSE	SELECT	switch	on PSU to	1,	
		-		Оы	erve th	at fire	indicati	on on CW	U is r	ot lit.
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		4	1.12.8.	2. Fire	Set (H	ad 1,	Side 1)	(contd.)		
				Set	PULSE	SELECT	Switch	on PSU to	2.	
li				Obs	erve th	at fire i	indicatio	on on CWL	j is no	tit.
				Set	PULSE	SELECT	siwtch	on PSU to	3.	
				Obs	erve th	at fire i	indicatio	on on CWL	J is no	e lit.
				Set	PULSE	SELECT	switch	on PSU to	4.	
				Obe	erve th	at fire i	ndicatio	on on CWL	J is lit	•
		4	1.12.8.	3. <u>Sho</u>	rt circu	it (Hea	1, Sid	• 1)		
				Dep		i hold s	hart circ	cuit button	on sa	nsitivity test
				Obe	erve th	ot fire i	indicatio	on on CWL	J extin	nguishes.
				Rele	ease sho	rt circu	it butto	n on PSU.		
				Obe	erve th	at fire i	indicatio	on on CWL	J re-li	ghts.
		4	1.12.8.	4. Fire	Roset (Head 1	, Side 1)		
	·			Set	PULSE :	SELECT	switch	on PSU to	3.	
				Obe	erve th	ot fire i	indicatio	on on CWL	J rema	ins lit.
				Set	PULSE	SELECT	switch	on PSU to	2.	
				Obs	erve th	et fire i	indicatio	on on CWL	J r em a	ine lit.
				Set	PULSE	SELECT	switch	on PSU to	1.	
				Obe	erve th	ot fire	indicati	on on CWI	J exti	nguishes.
				Retu	rn PUL	SE SELE	CT swit	ch on PSU	to 0.	ins extinguished.
		4	1.12.8.	5. Seni	itivity	and She	ort Circu	it Head C		_
				(SId	• 1, He	ods 2,	3, 4, 0	nd 8)		
										2, 3, 4 and 8
ISOUE	1		<u> </u>	by s	electin	inben 6	red head	on HEAD	SELEC	CT switch on PSU
	A			<u> </u>				 		
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QUALITY CONTROL DATA SHEET

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TITLE:

ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.12.8.6. Set Up for Side 2 Heads

Set all side 2 fault switches to OFF. Set all side I fault switches to ON. Set SIDE SELECT on PSU to side 2A. Set HEAD SELECT on PSU to head 1. Sat PULSE SELECT on 'SU to 0.

4.12.8.7. Fire Set (Head 1, Side 2)

Repeat 4,12,8,2.

4.12.8.8. Short Circuit (Head 1, Side 2)

Recest 4,12,8,3.

4.12.8.9. Fire Reset (Head 1, Side 2)

Repeat 4,12.8.4.

4.12.8.10. Sensitivity and Short Circuit Head Operation (Side 2, Heads 2,3,4, and 8)

> Repeat 4.12.8.2. to 4.12.8.4. for heads 2, 3,4 and 8 by selecting required head on HEAD SELECT switch on PSU.

4.12.8.11. Return HEAD SELECT switch on PSU to OFF.

4.12.9. 115V Power Failure

4.12.9.1. Set all side 1 and side 2 head FIRE AND FAULT switches to OFF. Depress and release reset switch on GSECU.

> Observe that system is functional as per paras. 4.3.1. and 4.3.2.

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ACCEPTANCE REQUIREMENT 83813-203 (SYSTEM A)	NTS FOR U.V.A.F.D			
4.12.9.2. <u>Si</u>	de 1 Power Failure			
Se	et SIA to OFF.			
	bserve that GSE 1 and	12, side 1 LE	DS o	n GSECU
	SE 1 and 2, side 2 LE .3.1.	DS continue (to fla	sh as per
C	arry out functional ter	t as per 4.3.	2.	
Se	et side 2, head 1 fire :	witch to ON	۱.	
0	beerve that CWU fire	lomp is lit.		
Se	ot side 2, head 1 fire:	witch to OFI	F.	
. 0	beerve that CWU fire	lamp extingu	ishes	•
S ₄	of SIA to ON.			
	de 2, GSE 1 and 2 LE er 4.3.1.	DS to continu	ve fla	ishing as
Si	de 1, GSE 2 LED to a	how continuc	us.	
4.12.9.3. <u>S</u>	et Up for Side 2 Power	Failure		
Se	et GSE made switch or	GSECU to I	N.	·
D	opress and release ress	et switch.		
	bserve that both side SECU light.	l and side 2 (GSE	LEDS ON
Se	et GSE mode switch or	GSECU to (out.	
D	epress and release ress	et switch.		
0	bserve that system ope	erates as per	4.3.1	
4.12.9.4. <u>Si</u>	de 2 Power Failure			

Set S2A to OFF.

Observe that GSE1 and 2 Side 2 LEDS on GSECU

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GRAVINER LIMITED, COLNBROOK, ENGLAND.

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QUALITY CONTROL DATA SHEET

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TITLE:

ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.12.9.4. Side 2 Power Failure (contd.)

extinguish.

GSE 1 and 2, side 1 LEDS continue to flash as per 4.3.1.

Carry out functional test as per 4.3.2.

Set side 1 head 1 fire switch to ON.

Observe that CWU fire lamp is lit.

Set side I head I fire switch to OFF. CWU fire lamp to extinguish.
Set S2A to ON.

Side 1 GSE 1 and GSE 2 LEDS to continue flashing as per 4.3.1.

Side 2 GSE 2 LED to show continuous.

Set SIA/S2A, S3 and S4 to OFF.

4.12.10. Response to Fire

4.12.10.1. Settings and Connections

Set Channel 1 and Channel 2 amplifiers on ascillascopes to 20V/cm.

Connect Channel 1 oscilloscope probe to side 1 ED terminal of HSIMU, and Channel 2 ascilloscope probe to side 2 ED terminal of HSIMU.

Connect probe return lines to pin 32 of monitoring point.

Connect pin 28 of monitoring point to external trigger input of oscilloscope using a X1 probe.

Set oscilloscope trigger mode to EXT. (positive edge).

Set trigger point at end of trace ensuring that end trace coincides with end of trace graticule.

Set time base to 0.2 secs/cm.

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	GRAVENER LIMITED, COLMOR	OOK, ENG	BLAND.	DATA SHEET No	G	15509
	QUALITY CONTROL DA	TA SH	EET	SHEET. No.	28	No. OF SHEETS
TITLE:	ACCEPTANCE REQUIREMENTS 53813-203 (SYSTEM A)	NTS FO	R U.V.A.F.D	.s. CONTRO	DL UN	4IT
	4.12.10.1.	Setting	and Connect	ions (contd.)		
			A/S2A, S3 and functions as pe		Obse	rve that
	4.12.10.2.	Respons	e to Fire (Set))		
		Note:	carried out a	bout 3 secon	ds oft	st should be er GSE 2 LEDS 2 have flashed.
			scilloscope trig ETECT TEST' o		depres	s and hold
		Note:	level in con	junction with ECT TEST' pu	repe	, adjust trigger at depressions tran , and re-
			e fire set tin		ffig.	٧.
	4.12.10.3.	Respons	e to Fire (Res	ot)		
		Note:	carried out a	bout 3 secon	de afte	est should be or GSE2 LEDS 2 have flashed.
		Select	negative edge	EXT trigger.		
		Re-arm	oscilloscops t	rigger.		
		Release	'FIRE DETEC	TEST' switc	h on (CWU.
			e oscilloscope Fig. 10.	waveform, t	roce i	o be of the
		Measur	e fire reset tin	ne t.		
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Set S1A, S2A, S3 and S4 to OFF. Remove oscilloscope probes. Switch off all power supplies. END OF TEST.

GRAYMER LIMITED, COLNBROOK, ENGLAND.

DATA
SHEET No. 95309
SHEET.No. 90 No. OF SHEETS

TITLE:

ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

SCHEDULE OF TESTS

APPENDIX I

Tost Definition	С	ategory			Pa	rometer	Values				Unit
4.1.		1 2 3			0.25	nax nax					Ohm
			Value 124V	420 Hz	Supply V1 = 2 V2 =	. = .9∨ .4∨	Value 102V	380 Hz	Supply V1 = V2 =	= 16V 3V	
			MI	M2	мз	M4	ΜΊ	M2	МЗ	M	
4.2.1.		1 2 3	-	-	140 148 160	1.25 1.45 1.65	-	•	100 106 115	1.1 1.3 1.55	mA Mass
	+-	1	140	140	85	0	115	115	45	0	
4.2.2.		2 3	150 165	150 165	89 97	0	123 135	123 135	.47 52	. 0	mA Max
4.4.		1 2	121 129	121 1 29	75 80	0	100 107	100 107	42 45	0	
4.4.		3	142	142	86	0	117	117	2 48	0	mA Mass
4.5.		1	146	146	270	0	118	118	176	0	
4.3.		2	156 171	1 56 171	280 295	0	126 138	126 138	185 198	0	mA Mas
			Value	of AC	Supply 2V 380	= Hz	Value	at AC	Supply 24V 420	a Hz	
4.73 4.74		1 2 3		5.7 ± 0 5.7 ± 0 5.7 ± 0).5).65			5.7 ± 5.7 ± 5.7 ±	0.5		Vol
4.75 4.76		1 2 3		322 ± 322 ± 322 ±	13 13			322 ± 322 ± 322 ±	10 12		Val
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GRAVINER LIMITED, COLNEROOK, ENGLAND.

QUALITY CONTROL DATA SHEET

DATA SHEET. No.

SHEET No. Q5509

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No. OF SHEETS

TITLE:

ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

SCHEDULE OF TESTS (contd.)

APPENDIX 1

Test Definition	Category	Paramete	er Values	Units
4.8.3.1.	1 2	0.63 ± 0.42		Second
4.8.3.2.	3	0.63 (+ 0.47 0.63 + 0.43 0.63 + 0.44		
		Side 1	Side 2	
4.8.6.2.	1 2 3	337 ⁺ 17 337 ⁺ 20 337 ⁺ 23	337 ⁺ 17 337 ⁺ 20 337 ⁻ 23	mS
4.8.6.3.	1 2 3	168 ⁺ 9 168 ⁻ 11 168 ⁻ 13	168 ⁺ 9 168 ⁻ 11 168 ⁻ 13	mS
4.8.9.	1 2 3	14.8 ± 0.74 14.8 ± 0.88 14.8 ± 1.03	14.8 ± 0.74 14.8 ± 0.88 14.8 ± 1.03	secon
4.8.10.	1 2 3	168 ⁺ 9 168 ⁺ 11 168 ⁺ 13	168 ⁺ 9 168 ⁺ 11 168 ⁺ 13	mS
4.9.2.	1 2 3	5.7 ± 0.45 5.7 = 0.5 5.7 = 0.65		Volts
4.9.3.	1 2 3	5.1 ± 0.6 5.1 = 0.68 5.1 = 0.85		Volts
4.9.4.	1 2 3	114.9 ± 0.6 114.9 = 0.7 114.9 = 0.8		Volts
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DATA SHEET No....

Q.5309

QUALITY CONTROL DATA SHEET

SHEET, No.

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

SCHEDULE OF TESTS (contd.)

APPENDIX 1

Test Definition	Category	Parameter \	Value	Units
4.10.2. 4.10.3. 4.10.4. 4.10.5.	1 2 3	27.5 ± 0.7 27.4 ± 0.9 27.2 ± 1.2		Volta
4.11.3.2. 4.11.3.3.	1 2 3	0.34 ± 0.035 0.34 ± 0.040 0.39 ± 0.050	0.39 ± 0.035 0.39 ± 0.040 0.39 ± 0.050	ae conc
4.11.3.5.	1 2 3	1.9 ± 0.5 1.9 ± 0.6 1.9 ± 0.8		second
4.11.6.	1 2 3	1.2 max 1.35 max 1.6 max	mA.	
4.11.7.1.	1) 2) 3)	GRUTIL V.4.		-
4.12.10.2	1 2 3	1.15 [±] 0.1 1.15 [±] 0.12 1.15 [±] 0.15		secon
4.12.10.3	1 2 3	0.68 ± 0.05 0.68 ± 0.06 0.68 ± 0.08		secon
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CLAYMIER LIMITED, COLNBROOK, ENGLAND.

DATA SHEET No. 0.5309......

SHEET. No.

No. OF SHEETS

QUALITY CONTROL DATA SHEET

CONTROL UNIT

ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. (53813-203 SYSTEM A)

APPENDIX 2

TITLE:

CALIBRATION OF PULSE SIMULATION BOX

1.0. EQUIPMENT REQUIRED FOR TESTS

28 V D.C. SUPPLY (0.5 AMP.). 2 x OSCILLISCOPE PROBES (x10) STORAGE OSCILLISCOPE (GOULD OS 4000 OR SIMILAR) PULSE SIMULATION BOX NORMALLY OPEN BIAS SWITCH

2.0. CONNECTIONS

CONNECT AS PER FIG. A

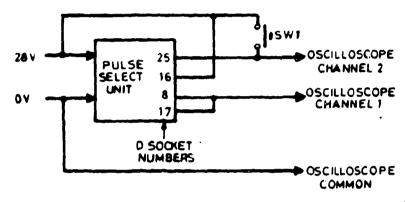


FIG. A

30 PULSE CHARACTERISTICS

3.1. SETTINGS

SET 28V D.C. SUPPLY TO 28V SET CHANNEL 1 Y AMP TO 1V/cm. SET CHANNEL 2 Y AMP TO 2V/cm. SET TRIGGER TO CHANNEL I NEGATIVE EDGE. SET'STORED TRIGGER POINT" TO 1/4 SCALE. SET TIME BASE TO 01 ms/cm. SET PULSE SIMULATION BOX PULSE SELECT SWITCH TO 4. SET OSCILLOSCOPE STORAGE MODE TO ROLL. SWITCH ON OSC'LLOSCOPE. SET CHANNEL I TRACE TO BE AT MID SCREEN. SET CHANNEL 2 TRACE TO BE ICM ABOVE BOTTOM OF SCREEN.

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GRAVINER LIMITED, COLNEROOK, ENGLAND.

DATA
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SHEET. No.

QUALITY CONTROL DATA SHEET

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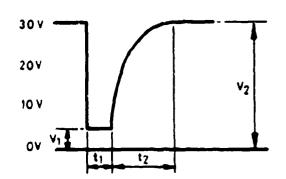
No. OF SHEETS

TITLE:

ACCEPTANCE REQUIREMENTS FOR U.V. A.F. D.S. CONTROL UNIT (53813-203 SYSTEM A)

3. 2. PULSE CHARACTERISTICS MEASUREMENT

SWITCH ON 28 V SUPPLY. ARM OSCILLOSCOPE TRIGGER. REPEAT DEPRESSION AND RELEASE OF BIAS SWITCH SW1 WHILST ADJUSTING TRIGGER LEVEL UNTIL WAVE FORM OF FIG, B IS OBSERVED. NOTE OSCILLOSCOPE SHOULD BE RE-ARMED AFTER EACH SWITCH DEPRESSION.



- V1 MAX.= 10V
- V1 MIN = 2 V
- V2 MAX.= 30 V
- V2 MIN. = 26V
- t1 MAX.= 300µS
- t1 MIN. = 50µS
- t2 MAX.= 800µS
- 12 MIN. = 100µS

FIG. B

WAVE FORM SHOULD BE WITHIN THE LIMITS OF FIG. B AS SHOWN.

- 4. 0. NUMBER OF PULSES
- 4. 1. SETTINGS

SET TRIGGER MODE TO CHANNEL 2 POSITIVE EDGE SET TIME BASE TO 10 m5/cm.

4. 2. OBSERVATION OF PULSES

ARM OSCILLOSCOPE, REPEAT DEPRESSION AND RELEASE OF BIAS SWITCH, WHILST ADJUSTING TRIGGER LEVEL, UNTIL WAVE FORM OF FIG.C IS OBSERVED.

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GRAVINER LIMITED, COLMBROOK, ENGLAND.	DATA SHEET NoQ53	
QUALITY CONTROL DATA SHEET	SHEET. No	No. OF SHEETS

TITLE :

ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S.
CONTROL UNIT (53813-203 SYSTEM A)

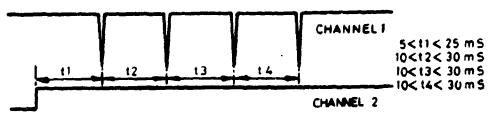


FIG. C

NOTE: DUE TO STORAGE CHARACTERISTIC OF OSCILLOSCOPE, PULSES MAY NOT BE UNIFORM IN HEIGHT. REPEAT DISPLAYS MAY BE NECESSARY TO ENSURE THAT ALL PULSES ARE PRESENT. WAVEFORM SHOULD BE WITHIN TOLERANCES SHOWN IN FIG. C

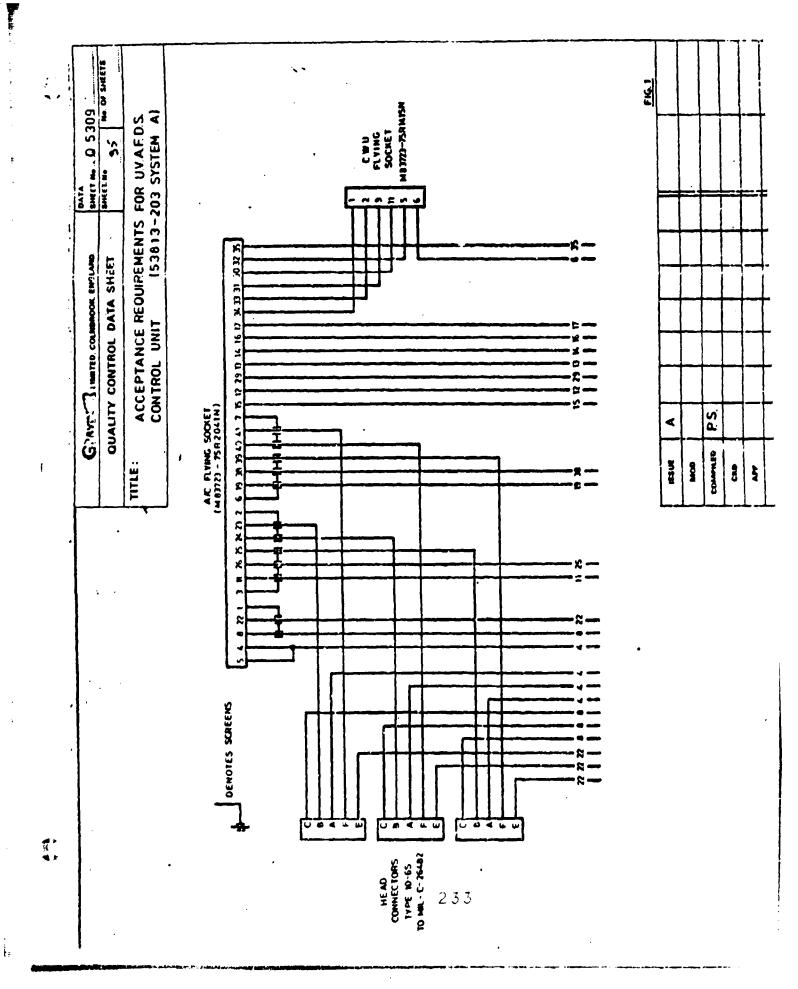
SET PULSE SELECT SWITCH ON PULSE SIMULATION BOX TO 3. OBTAIN OSCILLOSCOPE TRACE AS PREVIOUSLY, BY DEPRESSION OF SWI.

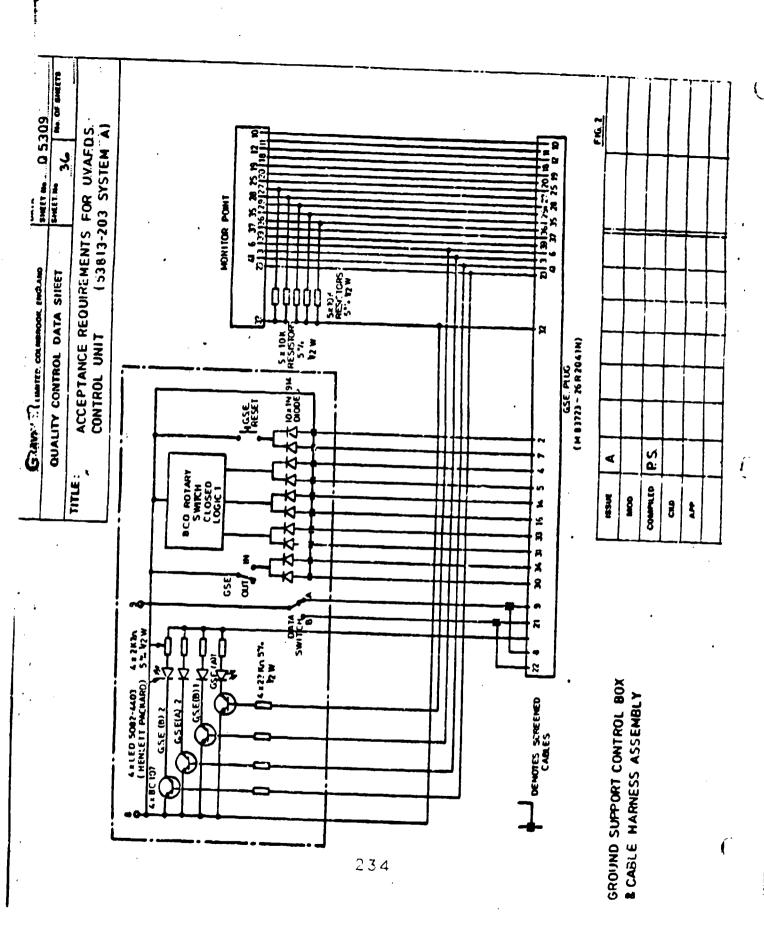
OBSERVE THAT 3 PULSES ONLY ARE PRESENT ON THE TRACE. THE RIGHT HAND PULSE OF FIG. C SHOULD NOW BE MISSING.

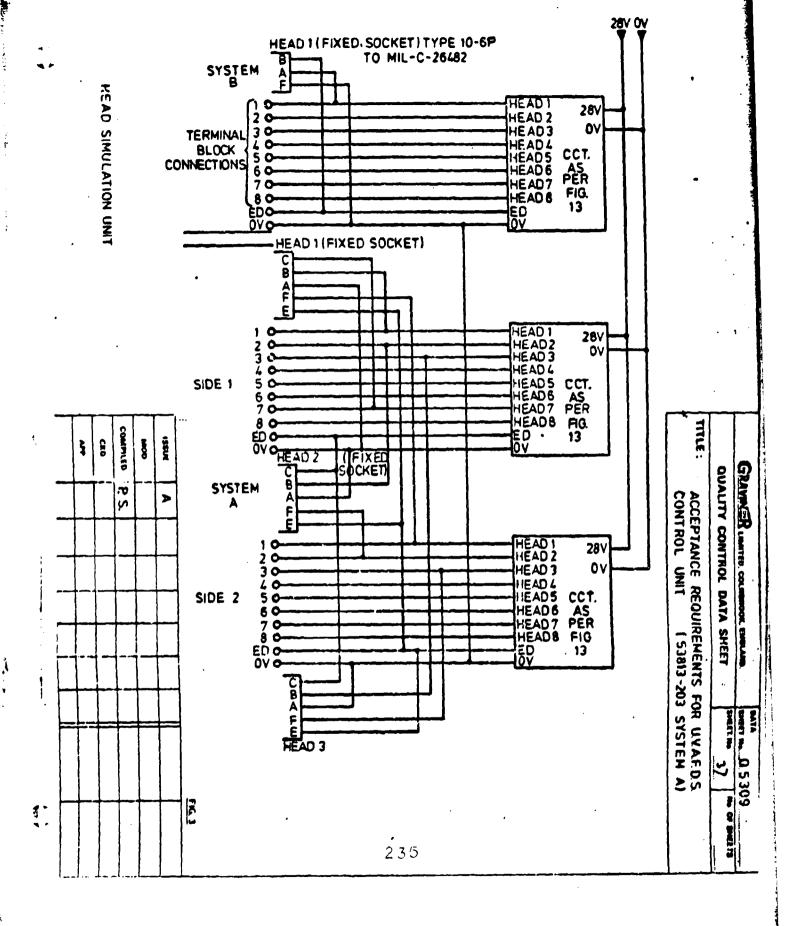
SET PULSE SELECT SWITCH TO 2,1 AND 0 AND OBSERVE CORRESPONDING NUMBER OF PULSES APPEARING ON THE OSCILLOSCOPE, WHILST UTILISING BIAS SWITCH AND OSCILLOSCOPE AS PREVIOUSLY.

SWITCH OSCILLOSCOPE AND 28 V SUPPLY OFF AND REMOVE TEST CONNECTIONS TO PULSE SIMULATION BOX.

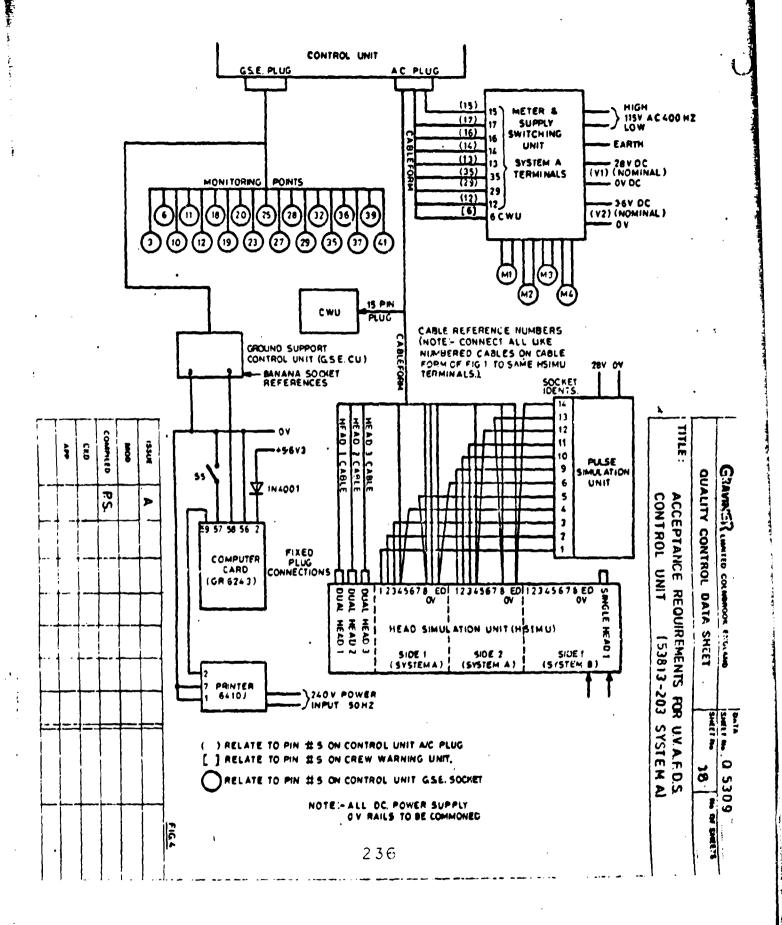
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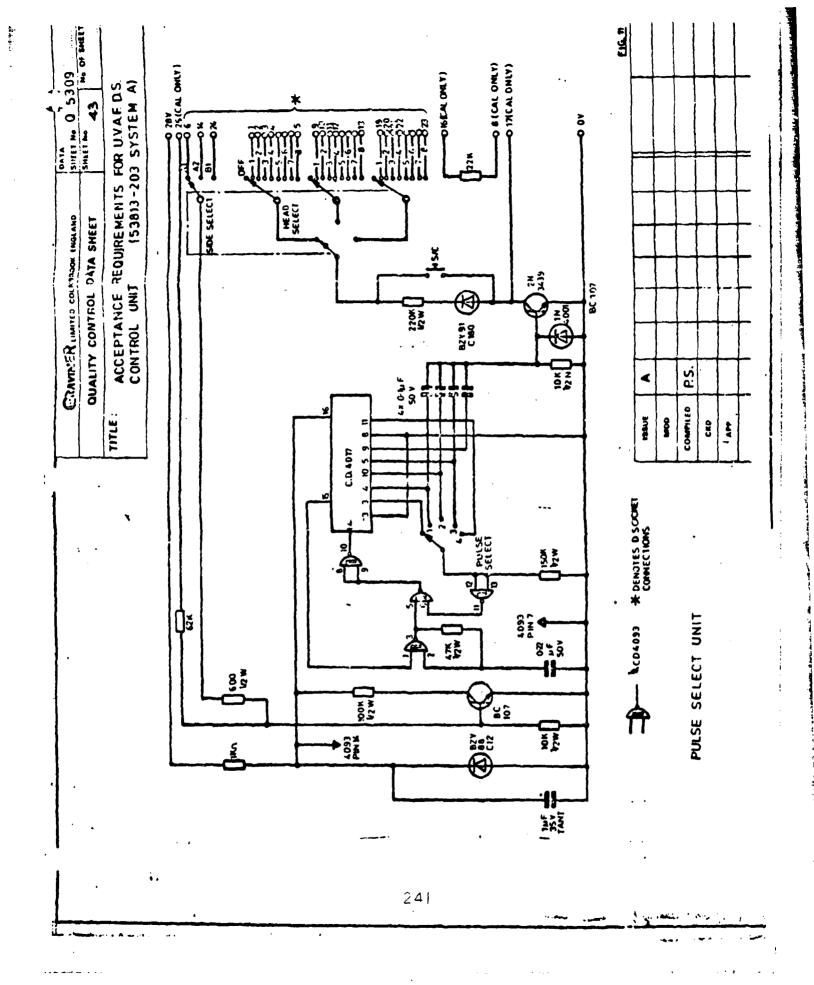
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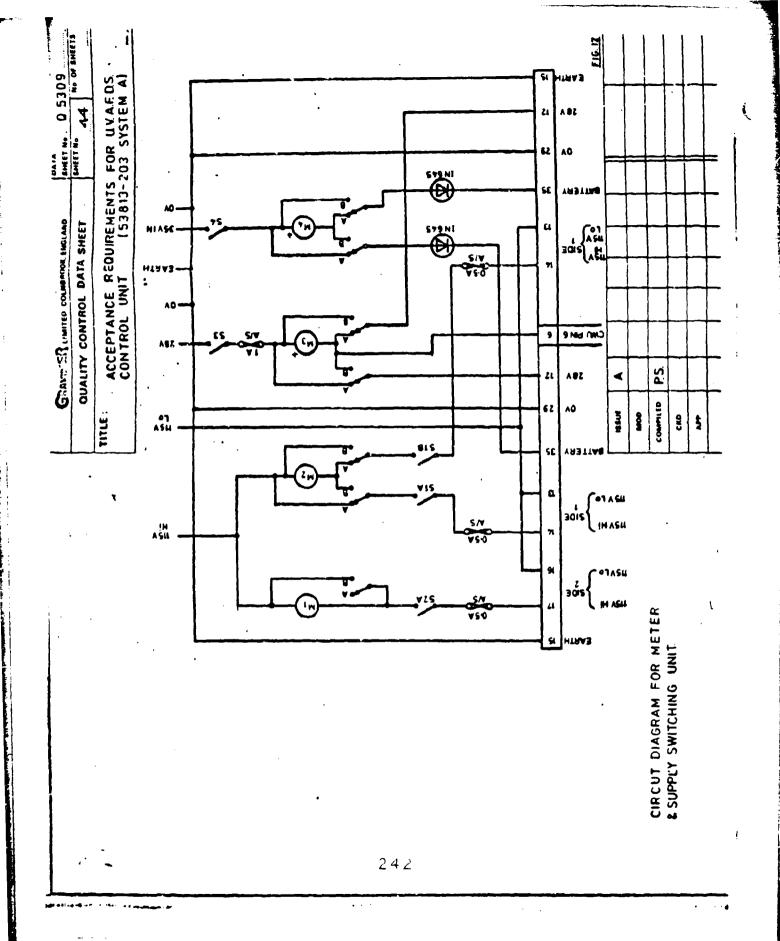
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		CONTROL D		SHEET, No. 40	No. OF SHEETS
TITLE:			REQUIREMENTS (53813	FOR U.V.A.F.	D. S.
	CH 2	->!86 33318 10111 20212 36313 46-14 56515 66516 70117 90611 90611 56516	P1 grus 10. 4 100 20304050647000300000000000000000000000000000000	AF IF 2F 3F AF SF SF SF SF SF SF SF SF SF S	ec 8
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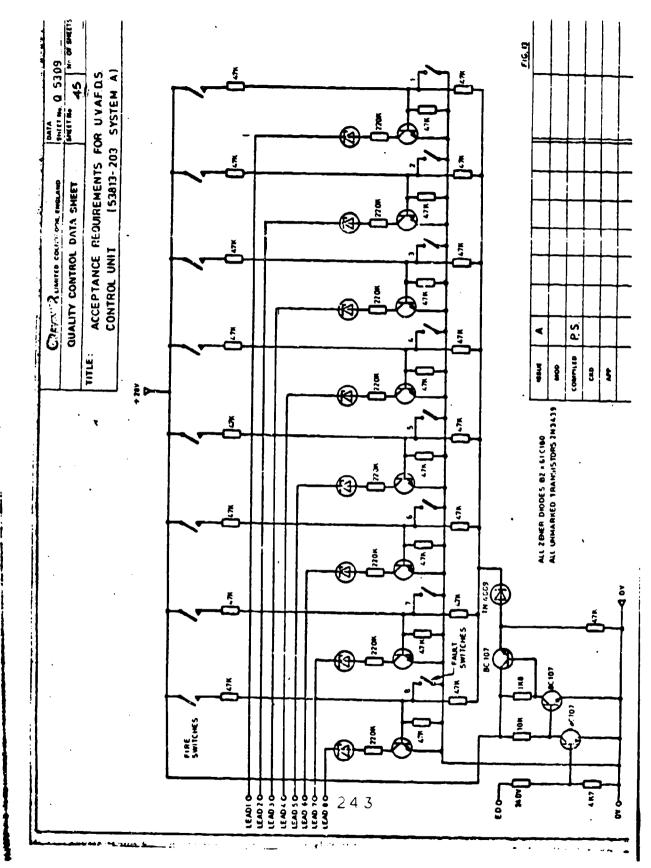
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TITLE:	ACC	EPTA	NCE	REO	UIRE!	MENTS 53813 -	FOR -203	U.V SYS	A.F. C)S. A)		
or	CH 1									ind Tr	of ace	
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	GRAYINER LIMITED, COLNEROOK, ENGLAND.	DATA SHEET No.	.5310
	QUALITY CONTROL DATA SHEET	SHEET, No.	No. OF SHEETS
TITLE:	ACCEPTANCE REQUIREMENTS FOR U.\ 53813-204 (SYSTEM B)	A.F.D.S. CON	TROL UNIT

Detinition

Q \$\$ 10 becomes a master document for functional performance testing of control unit 53813-204.

Performance values have been defined in compliance with "funnel or tiered telerances" philosophy and form the following categories.

- Type 1 Factory or Production Acceptance Limits apprepriate at normal ambient temperature conditions.
- Receiving Inspection or Customer Acceptance Limits Type 2 appropriate at normal ambient temperature conditions.
- Quality or Functional Acceptance Limits Type 3 appropriate at and between the declared extremes of operating temperatures.

In any repeat of test in two geographical areas there is expected to be some difference in test results. Differences within the stated accuracy of instrumentation and those due to acceptable variances based upon time dependency, transportation and test techniques are declared as acceptable. To meet these circumstances Type 1 limits used for Factory tests allow a smaller variation than those used for Type 2 limits by Receiving Inspection and as Customer Acceptance. These tests are cerried out at normal ambient temperature conditions.

Functional limits at extremes of operating conditions are determined and declared. From time to time quality audit tests may be carried out and performance characteristics are measured for compliance with values of the approval sample which are measured at appropriate extreme conditions, particularly with respect to temperature. Type 3 limits cater for functional acceptance characteristics and ollow a greater variation than Type 2 limits.

The correct acceptable value applicable to the nature of the test is detailed in a schedule and is to be selected for use as appropriate. Any test where a single value remains in the text is applicable to Type 1, 2, and 3 tests.

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				DATA SHEET	SHEET. No.	2	No. OF SHEETS
ritle :			ICE REQU (SYSTEM	JIREMENTS FOR U.V.	A.F.D.S. COP	NTROL	UNIT
(11)	Frequen	cy of Te	st .				
	The foll	owing te	nsts sholl (be carried out at a fre	quency appropri	ate to	definition.
	Type 1	All	units.				
	Type 2	•		anded that all units 'or ters procedures and sch	•	rpsed u	ently as
	Туре З	Init Intr Ces Intr	ietian of aduction setion of aduction	production. of a major modification production for three modification of new processes which by operator.	n . conths .	sd uctic	on standard.
(111)	Action	Required					
		For Type control (il results shell be reco	rded against Se	riol N	o. of each
				n abridged test report sh control unit is raise	•	obtoi	ned against
	lii (b)	For Type	l tests e	my follures shall be re	ported to the Di	ssign A	Authority.
		pe exam	o 3 tests, lined to le function.	any Centrel Unit Het fooste the perticular re	ails any test ar piacestie sub-a	part of	o test shall y causing
				resembly shall be rep and repeat testing carri			replocement
				ctory results on both no be released.	plecement sub-	assemi	olies, the
		the who	le betch,	re-test on either sub-o and rectification/desi can be released.	•		
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Pulse simulation unit as per FIG. 10. (Calibrated as per Appendix 2).

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TITLE	_		TANCE 204 (SY			ITS FOI	₹ U.V.	.F.D.S. (CONTROL	UNIT
<u>2</u> . <u>9</u>	CON	NECTI	ONS							
			ill suppl per FIC		set to (OFF. (Connect	cantrol un	it to suppl	ies and test
3.	NITI	AL SET	TINGS							
;	3.1.	•		•		•			Switching ng unit to	Unit to OFF. B.
;	3.2.	Rota	ry switch	n on GS	iE cont	rol unit	to posit	ion 6.		
•	3.3.	GSE	mode sv	vitch to	IN.					
;	3.4.	Date	switch	to A .						
;	3.5.	Com	puter ca	rd boud	r ate s	ettings	ю 30 0 С	:/sec.		
÷	3.6.	All H	read sim	ulation	unit, l	F1 (fire) and FA	(fault) sw	ritches to (OFF.
;	3 . 7.	M2 1	wt to 1	Amp rer	ge AC	•				
,	3.8.	M3 1	et to 1	Amp ra	nge D(C .				
	3.9.	M4 I	et to 10	mA roi	nge DC	•				
	3.10		g DVM : Hz (+ 0.		00v AC	range	switch d	on AC supp	oly and set	it to 124v
	3.11	. Usin	g DVM	set to 5	Ov DC	ronge S	iwitch a	n V ₁ and s	et it to 29	v ([±] 0.2v).
	3.12	. Usin	g DVM	et to 1	0√ DC	ronge s	witch or	V2 and s	et it to 4v	(± 0.1v).
	3.13	Swit		pply an	d set i				pod from V witch V3 s	3 supply. Supply off and
	3.14	. Head	d select	switch	on Puls	e simul	ation un	it to OFF.	•	
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·				ROL				8146	ET. No.	5	No. OF SHEETS
TITLE				LEQUIR TEM B)	EMENT	'S FOR	U.V.A	.F.D.S	. CON	TROL I	TINL
4.	TEST P	ROCED	URE								
	Notes	.1.		M ₄ sho			d at ea	ch test (and uni	ess stat	red otherwise
		2.	Limits	of all t	ests are	conta	ined in	Appendi	ix l.		
	4.1.	Earth	Conne	ctions							
											nce between
	4.2.	Prolin	ninery (Check (<u>) (H</u>	igh Sug	ply Vo	ltages)			
		4.2.1	Swi Swi	itch S4 itch S3	10 ON	, M4 al , M3 al	en bluor	rms to C ad less : ad less : FAIL" id	than than		mA. mA.
		4.2.2				-		that G			ide 1 of cotes.
			M ₂	to Indi	cete la	es than		mA.			
			Мз	to indi	coto le	es than		-mA.			
			M	to indi	cote z	ero.					
	4.3.	Prelin	ninory	Check (Dur						
		4.3.1	swi fia GS sec one	tch, of the state	an initial LED ide 1 C y 15 social CW	that Sid Plat off Dishould SSE2 Li cands. U right	de 1 GS period diffash d ED on G	of appro	begins eximate of app hould i	and co ily 4 se braicima flash ap	ntinues to conds. tely 3 per proximately
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		ANCE F 04 (SYS		EMENTS FOR	U.V.A.F	D.S. CON	TROL	UNIT
4.4.	4.3.2 Suppl	lam Reid Iam Des Fill Reid Fill	p to income 'fl p to existe 'fl exess 'fl te Dete ease 'fl te Dete	RE DETECT TE licate within on RE DETECT TE tinguish within AIL IND. TEST CT FAIL' lamp AIL IND TEST CT FAIL' lamp mining Mode	pproximo ST' push approxi ' push bu to show push but	itely one sec button on CV mately one su utton on CWU ton on CWU	ond. VU, 'R scand. J, Righ	ENG FIRE
	M ₂ to Note Obes M ₃ to	o indica : - m	ete less eter ned rage vo te less	thanthan than than than the the than the than the than the than the than the than the the than the the the than the the than the the the the the the than the	uate in sy	mpathy with	time s	hare.
4.5.	Depri obser M2 sl M3 sl M4 sl	one and we mete newld re hould re	hold CV or reading and less and less and zero	than	mA.	Herr' R ENG F	IRE' la	mps show
4.6.	Set so Set C Using V1 st V2 st	witches GSE MO DVM upply to upply to	SIB, So DE Swit set AC 16 volts 3 volts	out (Low Supp and S4 to Ol tch on GSECL supply to 102 is (= 0.2v), , (= 0.1v). inclusively, the	F. to IN. velts 380	Hz ([±] 0.5v)		F.
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GRAYMER LIMITED, COLNBROOK, ENGLAND.	BHEET No. Q 5310	
QUALITY CONTROL DATA SHEET	SHEET. No. 7 No. OF SHEET	8

ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

4.7. Regulator Operation

Note: All DC voltages are measure/with respect to pin 32 of manitoring points.

4.7.1. Settings (Low Supply)

Using DVM Set AC supply to 102V 360 Hz (=0.5v), V1 to 28 volts (=0.2V), V2 to 3.6 volts (=0.1v).

Set GSE Made Switch on GSECU to IN.

4.7.2. Set Switches 518, S3 and S4 to ON.

4.7.3. Regulation at Low Supply (5.6V Rail) Side 1

With DVM set at 10V range DC, check voltage at pin 12 of manitoring points. Voltage to be between ------volts minimum and ------ volts maximum.

4.7.4. Regulation at Low Supply (Head Supply) Side 1

BEWARE OF HIGH VOLTAGES ON THESE TERMINALS.

4.7.5. Settings (High Supply)

Using DVM set AC supply to 124V 420 Hz. Repeat 4.7.2. to 4.7.4. inclusively.

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ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

4.8. Timing Tests

4.8.1. Settings for power up time delay. With switches SIB, S3 and S4 set to OFF set AC supply to 400 Hz 115V.

> Set oscilloscope time base to 0.2 secs/cm, channel 1 and 2 amps. to 0.2V/cm, triggering to positive edge channel 1. Stored trigger point set to 1 trace.

Set channel 1 and 2 to DC made.

Set storage mode to ROLL.

Switch on oscilloscope and adjust channel I trace to be at mid-screen Adjust channel 2 trace to be 1/cm above bottom of screen. Set GSE made switch to IN.

4.8.2. Connections for power up Time Delay

Connect CH1 probe to terminal block manitoring point 23. Connect CH2 probe to terminal block monitoring point 12. All probe returns are connected to pin 32 of manitoring point.

Power Up Time Delay (Side 1) 4.8.3.

With oscilloscope trigger armed switch on system power 4.8.3.1 in the order S3, S4 and S1B.

> Note: If oscilloscope does not trigger, adjust trigger level in conjunction with setting SIA to OFF, re-arming trigger and setting SIB back to ON.

Observe oscilloscope waveform as per FIG. 5.

Measure time delay between rising edge of channel 1 and 2 as shown in FIG. 5.

Switch off S1B, S3 and S4 and remove ascillascope probes.

4.8.4. Settings for Time Share Timing

Switch on timer counter.

Set GSE mode switch to OUT.

Set timer for positive edge start, positive edge stop such that 500 mS can be measured.

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	ACCEPTAN 53813-204		REMENTS FOR U.V.A	.F.D.S. CON		JNIT					
	4.8.5.	Connection	ns for Time Share Timi	ing							
			imer probe to monitori un connected to monit								
	4.8.6.	Time Shor	• Timing								
	4.8.6.1. Set S18, S3 and S4 to ON. System to function as per 4.3.1.										
	4.8.6.2. Observe period of timer, time to be between										
	4.8.6.3. Resolect for negative edge stop and read timer. Time to be between secs. minimum end secs. maximum.										
	4.8.7. Cannections and Settings for Self Test Timer										
		Connect timer probe to manitering point pin 3. Select timer for positive edge start, positive edge stop. Select timing range to cover a 20 second pariod.									
	4.8.8.	Salf Test	Timing (Period)								
		•	period of timer, time to rescends anticimum.			secs. minimum					
	4.8.9.	Self Test	Timing (Duretion)								
	Reselect timer for positive edge start negative edge stop and observe period of timer. Time to be betweensecs. minimum andsecs. maximum. Remove timer probe connections.										
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ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM 8)

4.9. Ground Support Voltage Lines

Note: All DC voltages are manitored with respect to pin 32 of manitoring point.

4.9.1. Settings

With power on from previous test, set GSE Made Switch on GSECU to IN.

Depress and release reset button on GSECU.

Observe that GSE1 LED on Side 1 of GSECU lights.

4.9.2. Battery Monitoring Point

With DVM set to 10v range DC check voltage at pin 37 of manitaring point, voltage to be between ------ volts minimum and ------- volts maximum.

4.9.3. 115V Feed to GSE

NEWARE OF HIGH VOLTAGE ON THESE TERMINALS

Set DVM to read 200V AC range and connect probes to pins 10 and 11 of manitaring point.

Observe DVM reading, voltage to be between ------ volts maximum and ----- volts minimum.

4.10. Check Point Monitoring

4.10.1. Settings and Connections

Set GSE made switch to OUT on GSECU.

Depress and release reset switch on GSECU.

Set DVM to 50 volt range BC.

Connect DVM positive to pin 28 and negative to pin 32 of manitoring point.

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GRAYMER LIMITED, COLNBROOK, ENGLAND.

DATA SHEET No. Q 5310

QUALITY CONTROL DATA SHEET

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SHEET. No.

No. OF SHEETS

TITLE:

ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

4.10.2. Check Point 1

DVM reading to be zero volts.

Depress 'FIRE DETECT TEST' push button, 'R ENG FIRE' tamp to indicate, DVM reading to be between ------ volts minimum and ----- volts maximum.

4.10.3. Check Point 2

Repeat 4.10.2, with DVM positive connected to pin 29 of manitering points.

4.10.4. Check Point 3

Connect DVM to pin 35 of manitoring points.

DVM reading to be zero volts.

Depress 'FAIL IND TEST' push button, right 'FIRE DETECT FAIL' indication to show.

Observe DVM reading, voltage to be between ------ volts minimum and ----- volts maximum.

4.10.5. Check Point 4

Report 4.10.4, with DVM connected to pin 36 of manitoring points.

4.11. Ground Support Controlled Tests

4.11.1. RAM Test and Reset

Set GSE Mode switch on GSECU to IN.
Depress and release reset button on GSECU.
Observe that Side 1 GSE1 LED on GSECU rights.

4.11.2. Common Logic Test (Functional)

Select position 4 on rotary switch, depress and release reset button. Observe that Side 1 GSE 1 and 2 LED's on GSECU flash ON and OFF in the following sequence.

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ritle :		FANCE 204 (SYS		MENTS F	OR U.V.A	.F.D.S. CON		INIT
	4.1	1.2. <u>C</u> c	ommon La	ogic Test (Functional	(cointd.)		
		G	SE 2 51d	1 (ON-C	OFF), GSE	1 Side 1 (ON)	, GSE	2 Side 1 (ON)
		'R Ri _l pe	ENG Fight hand that	RE' lamp f 'FIRE DET	laches in sy ECT FAIL' 's are activ	f reset button, impathy with the lamp should re- re.	n first	flowh of GSE 2
	4.1	1.3. <u>C</u>	ommon L	ogic Test (Timing)			
		4.	11.3.1.	Connection	ins and Set	ings		
				Set trigge Set displa Set time b	r to CH1 (p y made to (less to 0.1		·	0.2V/cm.
				Connect C	hannel 2 p	robe to pin 23 robe to pin 3 o lines to pin 3	of manie	toring point.
		4.	11.3.2.	Side 1 Tin	ning of Con	nmon Logic Tes	<u>t</u>	
				Arm oscill Depress or Wave form	ig and S4 to accape trig nd release in a to be as f	iger. Peest button on	GSECI	J.
				conjunction rearming of Take mean	on with dep of oscilloss wroments o	not trigger, ad treation of GSE ape trigger. I ty and tz.		
				Remove or	cilloscope	probes.		
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DATA SHEET No.

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QUALITY CONTROL DATA SHEET

SHEET. No.

No. OF SHEETS

TITLE:

ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

4.11.4. Background Programme Test

Select position 5 on GSECU retary switch. Depress and release reset button. After 5 seconds no LED's to show on GSECU.

4.11.5. Idle Programme Test

Select position 0 on GSECU rotary switch.

Depress and release reset button.

Observe that side 1 GSE1 and 2 LED's on GSECU show.

4.11.6. Data Retention Test

Set S4 to OFF. Select position 2 on GSECU rotary switch, degrees and release reset button.

Observe that side 1 GSE1 LED on GSECU lights.

Select position 3 on GSECU rotary switch, depress and release reset button.

Observe that side 1 GSE1 and GSE2 LED's on GSECU lights.
Reselect position 2 on GSECU rotary switch, depress and release reset button.

Observe that side I GSEI LED on GSECU lights.

Set \$18 and \$3 to OFF. Wait 30 seconds.

Select position 3 on GSECU rotary switch .

Set SIB and S3 to ON.

Observe that only side 1 GSE1 LED on GSECU lights.

Resolect position 2 on GSECU rotary switch.

Set S4 to ON.

Depress and release reset button on GSECU. Observe that only Side 1 GSE1 LED on GSECU lights.

Set S1B and S3 to OFF. Wait 30 seconds.

Select position 3 on GSECU rotary switch. M4 to read between ----- mA minimum and ------ mA maximum.

Set S18 and S3 to ON. Observe that side 1 GSE1 and GSE2

LED on GSECU light.

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ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

4.11.7. Data readout Test

Switch on V3 (supply to computer card). Switch an mains power to printer.

Select position 2 on GSECU rotary switch.

Depress and release reset switch on GSECU.

Observe that Side 1 GSE 1 LED on GSECU lights.

Select position 1 on GSECU rotary switch. Depress and hold reset switch on GSECU.

Depress and release \$5.

Observe that printer prints -----

Release reset switch on GSECU.

Printer should print as per FIG.7.

When printer stops observe that GSE 1 LED (Side 1) on GSECU lights.

4.12. System Function Tests

All fire and fault indications refer to 'R ENG FIRE' and right hand 'FIRE DETECT FAIL' lamps on CWU.

Note:

These tests are carried out using the head-simulation unit referred to as HSIMU.

All references to Side 1 fault and fire switches refer to system B side 1. System A fault and fire switches are not used.

4.12.1. Initialise for Functional Tests

With system still powered from previous tests select position 6 on rotary switch of GSECU.

Set GSE made switch to OUT.

Depress and release reset switch on GSECU. Observe that system functions as per 4.3.1.

4.12.2. Set side I head I fire switch to ON.

Fire indication on CWU to show.

Set side 1 head 1 fire switch to OFF.

Fire indication on CWU to extinguish.

Repeat 4,12,2, for heads 2, 3, 4, and 8.

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TITLE:

ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

4.12.3. Failed Heads

Set side 1 heads 5, 6 and 7 fault switches on HSIMU to ON.
Set side 1 heads 1, 3 and 4 fault switches on HSIMU to ON.
Observe that right hand 'FIRE DETECT FAIL' lamp does not light at next occurrence of GSE 2 (side 1) LED's flashing on GSECU.
Set side 1 heads 1, 3 and 4 fault switches on HSIMU to OFF.
Set side 1 heads 2 and 8 fault switches on HSIMU to ON.
Observe that right hand 'FIRE DETECT FAIL' lamp does not light at next occurrence of GSE2 (Side 1) LED flashing on GSECU.

4.12.4. Adjacency Set Failure

4.12.4.1. Heads 1 and 2 Adjacency Set

Set side 1 heads 1, 2, 3, 4 and 8 fire and fault switches to OFF. Set GSE mode switch on GSECU to IN. Depress and release reset button. Observe that side 1 GSE 1 LED on GSECU lights. Set head I and 2 fault switches on side I to ON. Set GSE made switch on GSECU to OUT. Depress and release reset button. Right hand CWU 'FIRE DETECT FAIL' lamp should light immediately after the first occurrence of GSE 2 (Side 1) LED floshing on GSECU. Set head I and 2 fault switches on side I to OFF. After the occurrence of the next flushing sequence of GSE 2 LED's (occurring approximately once every 15 seconds) observe that right hand 'FIRE DETECT FAIL' lamp does not extinguish.

4.12.4.2. Heads 2 and 3 Adjacency Set

Repeat 4.12.4.1. using heads 2 and 3 fault switches.

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TITLE:	ACCEPTANCE REQUIREMENTS FOR U.V. 53813-204 (SYSTEM B)	.A.F.D.S. CONTROL	UNIT

4.12.4.3. Heads 4 and 8 Adjacency Set

Repeat 4.12.4.1. using heads 4 and 8 fault switches. Set GSE made switch to IN. Depress and release GSE reset switch.

4.12.5. Short Circuit Head Operation

4.12.5.1. Set Up

Set system B fault switches to OFF.

Check that all system B side 1 fire switches are set to OFF.

Set SIDE SELECT switch on pulse select unit (PSU) to side 1B.

Set HEAD SELECT switch on pulse select unit to head 1.

Set PULSE SELECT switch on PSU to 0.

Set GSE made switch on GSECU to OUT.

Depress and release reset switch on GSECU.;

Observe that system functions as per 4.3.1.

4.12.5.2. Fire Set (Head 1)

Note:

Allow 2 seconds at each switch position before abserving result on CWU.

Set PULSE SELECT switch on PSU to 1.

Observe that fire indication on CWU is not lit.

Set PULSE SELECT switch on PSU to 2.

Observe that fire indication on CWU is not lit.

Set PULSE SELECT switch on PSU to 3.

Observe that fire indication on CWU is not lit.

Set PULSE SELECT switch on PSU to 4.

Observe that fire indication on CWU is lit.

		 	 	 	
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TITLE:	ACCEPTANCE REQUIREMENTS FOR UVAF	DS CONTROL UNIT	53813-204

4.12.5.3. Short Circuit (Head 1)

Depress and hold short circuit button on pulse simulation unit.

Observe that fire indication on CWU extinguishes.

Release short circuit button on PSU.

Observe that fire indication on CWU re-lights.

4.12.5.4. Fire Reset (Head 1)

Set PULSE SELECT switch on PSU to 3.

Observe that fire indication on CWU remains lit.

Set PULSE SELECT switch on PSU to 2.

Observe that fire indication on CWU remains lit.

Set PULSE SELECT SWITCH on PSU to 1.

Observe that fire indication on CWU extinguishes.

Return PULSE SELECT switch on PSU to 0.

CWU fire indication to remain extinguished.

4.12.5.5. Sensitivity and Short Circuit Head Operation (Heads 2, 3, 4, 8)

Repeat 4.12.5.2. to 4.12.5.4. for heads 2, 3, 4 and 8 by selecting required head on HEAD SELECT switch on PSU.

4.12.5.6. Set S1B, S3 and S4 to OFF.

Set head select switch on PSU to OFF.

4.12.6. Response to Fire

4.12.6.1. Settings and Connections

Set shannel 1 amplifier an ascillascope probe to 20v/cm.

Connect channel 1 ascillascope probe to System 8 side 1.

ED terminal of HSIMU,

Connect probe return to pin 32 of manitoring point.

Connect pin 28 of manitoring point to external trigger input of ascillascope, using X1 probe.

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		4.	12.6.1	. <u>Settin</u>	ge and	Connec	tions (ca	mtd.)		
				Set tri	gger po	int at	-	oce en	wring	itive edge). that end trace
				Storag Set \$1	e mode	set to ind \$4 t			ve tha	t system function
		4.	12.6.2	. Respor	se to f	1re:(5e)	<u>)</u>			
					3 1000		-			e carried out U (side 1)
							gger on on CW		7 94 4 G	nd hold 'FIRE
				conjur	nction i	vith rep	eat dep	ressi ans	of 'FI	igger level in RE DETECT TES witch depression
				_	form she t time		f the for	m of Fl	G. 8.	Measure
		4.	12.4.3	. Respor	nse to F	ìre (Rei	et)			
				trigge Releas	r. 10 'FIRE ve osci	DETEC	T TEST	switch	on CV	ive edge EXT VU. be of the form
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ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-20#(SYSTEM B)

SCHEDULE OF TESTS

APPENDIX 1

Test Definition	Category			Parameter	Values			Units		
4.1.	1 2 3		0.2 0.25 0.3 m	max				Ohm		
		Values at / 124V 420	AC Supp Hz V1 V2	= 29∨	Values at A 102V 390 H	z VI	y = = 16V = 3V			
4.2.1.	1 2 3	M2	M3 140 148 160	M4 1.25 1.45 1.65	M2 - -	M3 100 106 115	M4 1.1 .1.3 1.55	mA Max.		
4.2.2.	1 2 3	140 150 165	85 89 97	0 0	115 123 135	45 47 52	0 0	mA Max.		
4.4.	1 2 3	121 129 142	75 80 86	0	100 107 117	42 45 48	0 0 0	mA Max.		
4.5.	1 2 3	146 156 171	270 280 295	0 0 0	118 126 138	176 185 198	0	mA Max.		
		Values at	102V	dy = 380 Hz	Value	124 V	Supply = 420Hz			
1.23	2 3	5.7 ± 5.7 ±	0.45 0.5 0.65			5.7 ± 0.45 5.7 ± 0.5 5.7 ± 0.65				
4.74	2 3	322 ± 322 ± 322 ±	35 37 37			322 322 322	10 12 17	Volts		
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ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-20\$ (SYSTEM B)

SCHEDULE OF TESTS (Contd.)

APPENDIX 1

Test Definition	Category	Parameter	Value	Uni
	1	337 + 1		†
4.8.6.2.	2	337 🚼 20	0	mS
	3	337 ± 2	3	
	1	168 + 9		
4.8.6.3.	2	168 🗓 1	1	mS
	3	168 - 13		
	1	14.8 7		
4.8.8.	2	14.8 🛨 (0.88	500
	3	14.8 -	1.03	1
	1	168 - 9		
4.8.9.	2	168 🛨 1		mS.
	3	168 = 13	3	1
	1	5.1 ± 0	.6	
4.9.2.	2	5.1 ± 0 5.1 = 0	.48	Val
	3	5.1 - 0	.85	
	1	114.9		
4.9.3.	2 3	114.9		Val
	3	114.9	0.8	
4.10.2.	1	27.5 [±]	9.7	
4.10.3.	2	27.4 -	0.9	Vol
4.10.4.	3	27.2 ±	1 2	ł
4.10.5.	,	2/.2 -	1.4	
		6 1	12	
	1	0.37 - 0.035	0.39 + 0.035	7
4.11.3.2.		0.39 - 0.04	0.39 ± 0.04	-
	3	0.39 - 0.05	0.34 - 0.05	
. s. 5.1.	2	0.63 ±	0.42 0.43 0.63/-0.44	500
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SCHEDULE	OF TESTS (Co	APPENDIX 1						
Test Definition	Category	Parameter Val			Units			
4.11.6.	1.11.6. 1 1.2 max. 2 1.35 max. 3 1.6 max							
4.11.7.1.	1) 2) 3)	GRUTIL V	.4		•			
4.12.6.2.	1 2 3	0.85 ⁺ 0.1 0.85 ⁺ 0.12 0.85 ⁺ 0.15			secor			
4.12.6.3.	1	0.69 - 0.05 0.69 - 0.06			1000			
	3	0.48 - 0.06						
APPENDIX	3 SCHEDULE	0.46 - 0.06						
APPENDIX	3	0.48 ± 0.06 OF TESTS 3.6 ± 0.6 3.6 ± 0.65			veits			
	3 SCHEDULE	0.48 ± 0.08 OF TESTS 3.6 ± 0.6						
4.7.	3 3 SCHEDULE 1 2	0.48 ± 0.06 OF TESTS 3.6 ± 0.6 3.6 ± 0.65			veits			
4.7.	3 3 SCHEDULE 1 2	0.48 ± 0.06 OF TESTS 3.6 ± 0.6 3.6 ± 0.65			veits			
4.7.	3 3 SCHEDULE 1 2 1 2	0.48 ± 0.06 OF TESTS 3.6 ± 0.6 3.6 ± 0.65			veits			
4.7.	3 3 SCHEDULE 1 2	0.48 ± 0.06 OF TESTS 3.6 ± 0.6 3.6 ± 0.65			veits			
4.7. 4.9.	3 3 SCHEDULE 1 2 1 2	0.48 ± 0.06 OF TESTS 3.6 ± 0.6 3.6 ± 0.65			veits			
4.7. 4.9.	3 3 SCHEDULE 1 2 1 2	0.48 ± 0.06 OF TESTS 3.6 ± 0.6 3.6 ± 0.65			veits			

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	3.6.	Usia 400	ng DVM Hz (-	et to 0.5√).	500V A	C range	:, witci	on AC	supply (and set	it to 115V
	3.7.	Unit	ng DVM	set to	50 V DC	: renge,	switch	un VI ar	nd set it	10 2 8	V DC (=0.2V
	3.8.	. Ines	rt batte	ry cord	into co	u l ortn a	nit 5381.	3-204.			
4.0.	Proc	odure.									
	4.1.	Set	\$3 to C	N.	Obe	erve the	et R.he	nd 'FIRE	DETEC	TFAIL	' lamp lights.
	4.2.	Wei	t for ½ l	nour to			to charge				
	4.3.		S1B to								
			ierve thi L'iomp			1 LED c	n GSEC	U lights	and R	, hand '	FIRE DETECT
	4.4.	Set	rotery s	witch o	n GSE			ss and re CU light		eet but	ton on GSEC
	4.5.	Set	518 and	53 to	OFF.						
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DATA SHEET No. 0.53 LO

SHEET. No

QUALITY CONTROL DATA SHEET

2

No. OF SHEETS

TITLE:

ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S.
CONTROL UNIT (53813-204 SYSTEM B)

APPENDIX 2

CALIBRATION OF PULSE SIMULATION BOX

1.0. EQUIPMENT REQUIRED FOR TESTS

28 V D.C. SUPPLY (0.5 AMP.).
2 x OSCILLISCOPE PROBES (x10)
STORAGE OSCILLISCOPE (GOULD OS 4000 OR SIMILAR)
PULSE SIMULATION BOX
NORMALLY OPEN BIAS SWITCH

2.0. CONNECTIONS

CONNECT AS PER FIG. A

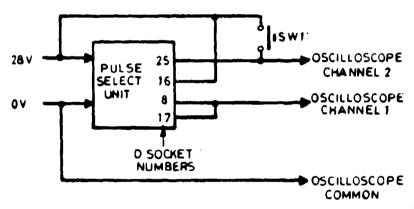


FIG. A

3.0. PULSE CHARACTERISTICS

3.1. SETTINGS

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SET 28V D.C. SUPPLY TO 28V

SET CHANNEL 1 Y AMP TO 1V/cm.

SET CHANNEL 2 Y AMP TO 2V/cm.

SET TRIGGER TO CHANNEL 1 NEGATIVE EDGE.

SET **STORED TRIGGER POINT** TO **1/4 SCALE.

SET TIME BASE TO 0.1 mS/cm

SET PULSE SIMULATION BOX PULSE SELECT SWITCH TO 4.

SET OSCILLOSCOPE STORAGE MODE TO ROLL.

SWITCH ON OSCILLOSCOPE.

SET CHANNEL 1 TRACE TO BE AT MID SCREEN

SET CHANNEL 2 TRACE TO BE I cm ABOVE BOTTOM OF SCREEN

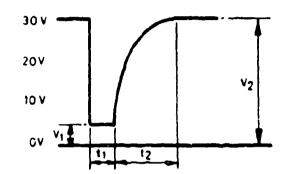
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ACCEPTANCE REQUIREMENTS FOR U.V. A.F. D.S. CONTROL UNIT (53813-204 SYSTEM B)

3. 2. PULSE CHARACTERISTICS MEASUREMENT

SWITCH ON 28 V SUPPLY. ARM OSCILLOSCOPE TRIGGER. REPEAT DEPRESSION AND RELEASE OF BIAS SWITCH SW! WHILST ADJUSTING TRIGGER LEVEL UNTIL WAVE FORM OF FIG. B IS OBSERVED. NOTE OSCILLOSCOPE SHOULD BE RE-ARMED AFTER EACH SWITCH DEPRESSION.



V1 MAX.= 10V V1 MIN. = 2V V2 MAX.= 30V V2 MIN. = 26V t1 MAX.= 300µS t1 MIN.= 50µS t2 MAX.= 800µS t2 MIN.= 100µS

FIG. B

WAVE FORM SHOULD BE WITHIN THE LIMITS OF FIG. B AS SHOWN.

4. O. NUMBER OF PULSES

4. 1. SETTINGS

SET TRIGGER MODE TO CHANNEL 2 POSITIVE EDGE SET TIME BASE TO 10 mS/cm.

4. 2. OBSERVATION OF PULSES

ARM OSCILLOSCOPE, REPEAT DEPRESSION AND RELEASE OF BIAS SWITCH, WHILST ADJUSTING TRIGGER LEVEL, UNTIL WAVE FORM OF FIG.C IS OBSERVED.

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SHEET NO. Q 5310

QUALITY CONTROL DATA SHEET

SHEET. No.

No OF SHEETS

TITLE:

ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S.
CONTROL UNIT (53813-204 SYSTEM B)

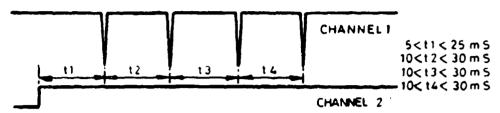


FIG. C

NOTE: DUE TO STORAGE CHARACTERISTIC OF OSCILLOSCOPE, PULSES MAY NOT BE UNIFORM IN HEIGHT. REPEAT DISPLAYS MAY BE NECESSARY TO ENSURE THAT ALL PULSES ARE PRESENT. WAVEFORM SHOULD BE WITHIN TOLERANCES SHOWN IN FIG. C

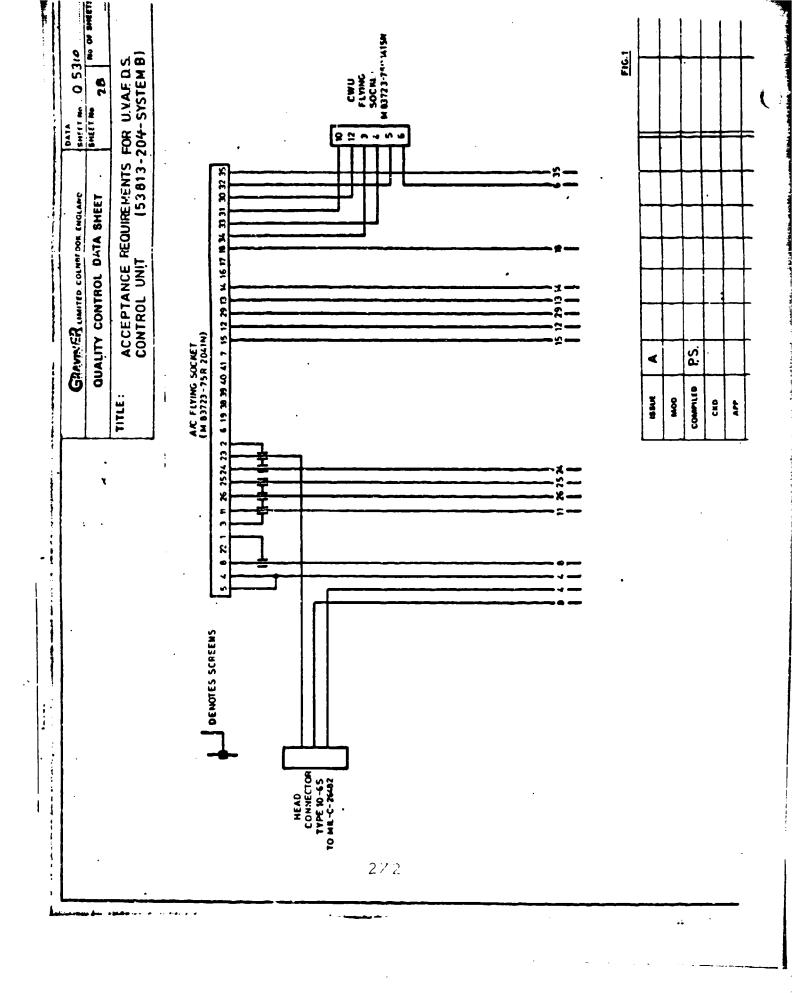
SET PULSE SELECT SWITCH ON PULSE SIMULATION BOX TO 3. OBTAIN OSCILLOSCOPE TRACE AS PREVIOUSLY, BY DEPRESSION OF SW1.

OBSERVE THAT 3 PULSES ONLY ARE PRESENT ON THE TRACE. THE RIGHT HAND PULSE OF FIG. C SHOULD NOW BE MISSING.

SET PULSE SELECT SWITCH TO 2,1 AND 0 AND OBSERVE CORRESPONDING NUMBER OF PULSES APPEARING ON THE OSCILLOSCOPE, WHILST UTILISING BIAS SWITCH AND OSCILLOSCOPE AS PREVIOUSLY.

SWITCH OSCILLOSCOPE AND 28 V SUPPLY OFF AND REMOVE TEST CONNECTIONS TO PULSE SIMULATION BOX.

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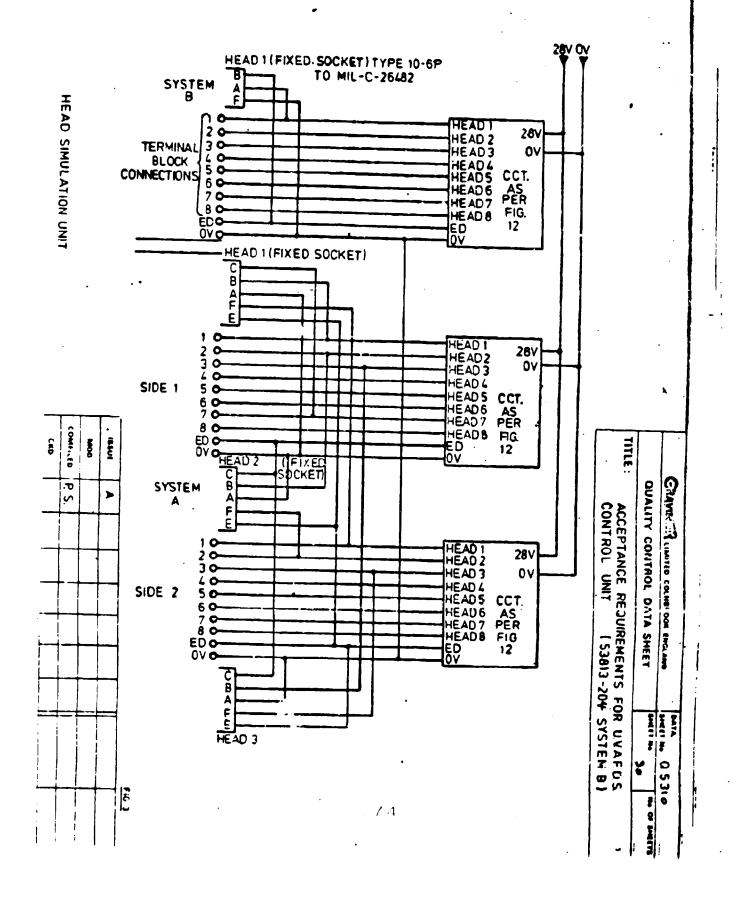
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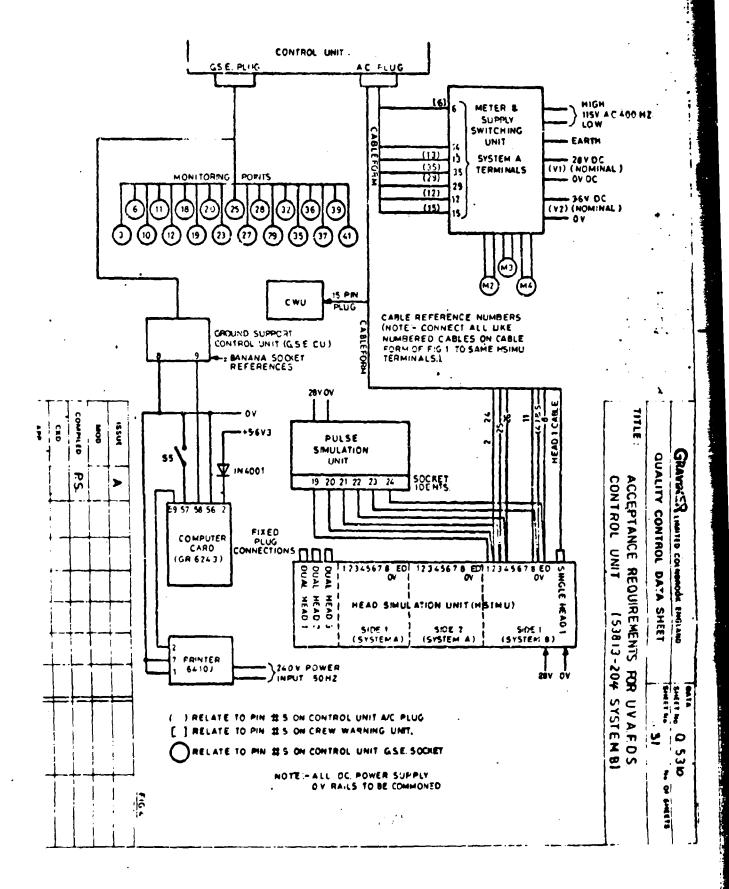
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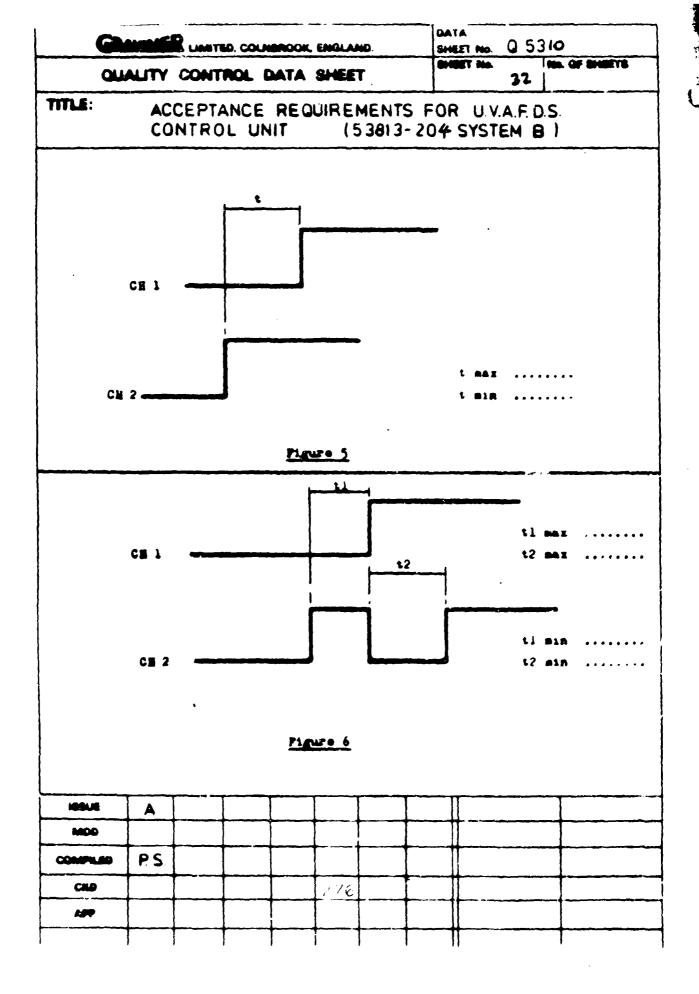
GROUND SUPPORT CONTROL.BOX & CABLE HARNESS ASSEMBLY

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GRAVINER LIMITED, COLNBROOK, ENGLAND.

SHEET No. Q 5310

SHEET. No.

QUALITY CONTROL DATA SHEET

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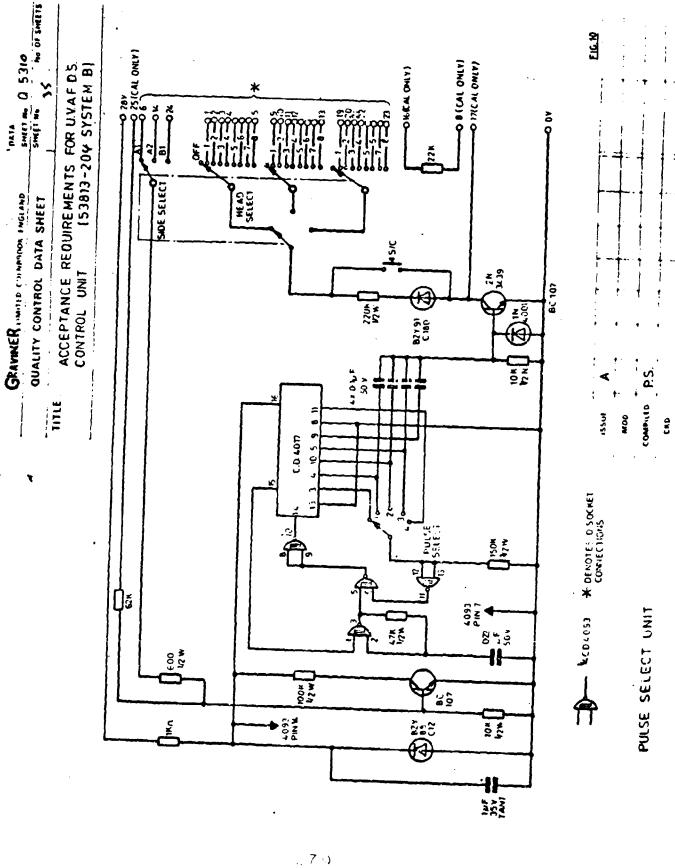
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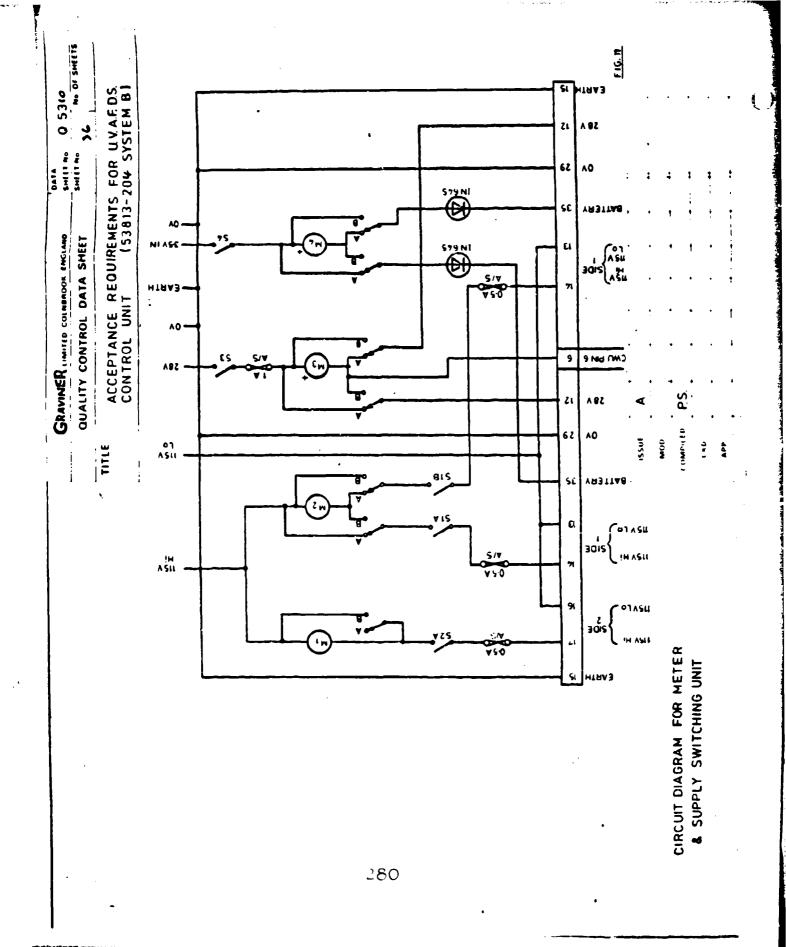
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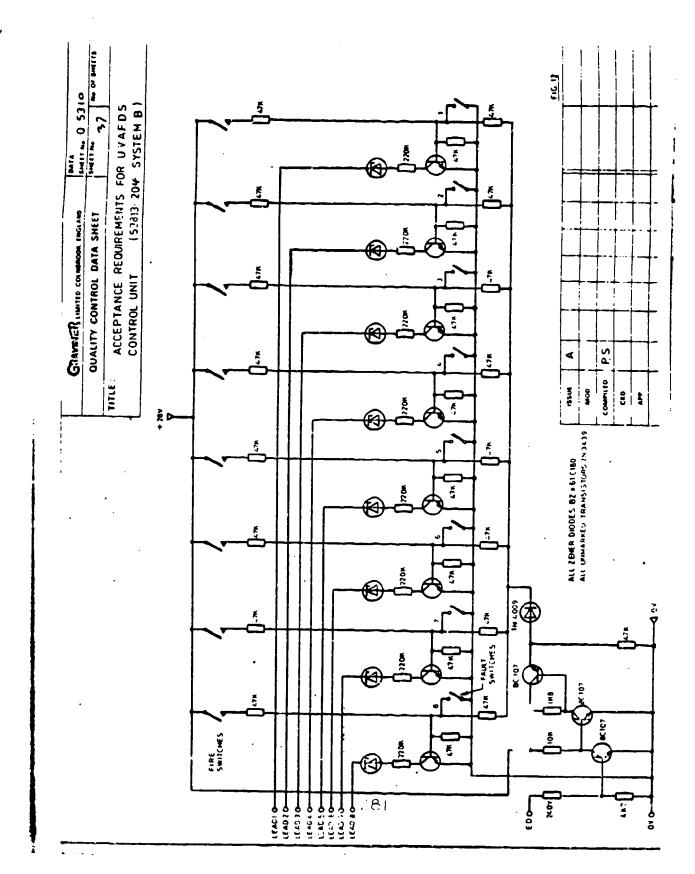
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APPENDIX B-2

APPROVAL TEST SCHEDULE ATS 52

GRAVINER LIMITED

ATS.No.52

Test Schedule
for
Ultra-Violet
Advanced Fire Detection System

985 Compiled by.

APPROVALS ENGINEER.

DATE. 26.5.78.

Test Schedule for

Ultra-Violet

Advance Fire Detection System

Amendment Record

Issue No.	Page No.	Para.No.	Amendment	Date
1			Introduction	26.5.78.
2 .	Part 1			27.6.78.
	Part 2) Revised	
	Part 3))	
	1	4.2.1.	Added	
		4.2.2.	Added	
	2	4.3.4.	Revised	
3	Part 1) Reference to TSO-C11(d) deleted.	11.1.79.
	Part 3) TSO-C79 edded.	
	Part 4	Para.4.5.3.	()	
4	Part 4	Para.4.4.	Revised	26.3.79.
		Pera.4.6.	Test Plan added.	
5	Part 4	A11	Revised	10.9.79.
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CONTENTS

PART 1. Related Documents

PART 2. Description

PART 3. Test Equipment

PART 4. Test Schedule

PART 1.

List of related documents applicable to this schedule

SOR.078104	General Dynamics. Statement of Work.
MIL-STD-810C	Environmental Test Methods.
MIL-STO-461	Electromagnetic Interference Requirements.
MIL-D-27729A	Detecting Systems, Flame and Smoke, Aircraft and Aerospace Vehicles.
MIL-W-25038B	Wire, Electrical, High Temperature and Fire Resistant. Aircraft.
TS0.C79	Fire Detectors Radiation Sensing Type
MIL-STD-704A	Electric Power Aircraft; characteristics and utilisation of.

PART 2

Description

The Ultra Violet Advanced Fire Detection System is intended for use in high performance aircraft to detect engine/nacelle fires.

The multi-channel system comprising, Computer Control Unit (C.C.U.), Crew Warning Unit (C.W.U.) and up to 8 Detector Units shall detect aircraft engine/necelle fires within one second.

Two systems are proposed :

System 'A' shall include the following features :-

Automatic Self Test Fault Discrimination Capability Fault Maintenance Read Out and Manual Confidence Test.

The simplified System 'B' shall incorporate Manual Test only.

PART 3

Test Equipment

The following test equipment shall be used where necessary to carry out the tests as detailed in Part 4 of this schedule.

Temperature and Humidity tests shall be carried out using "Montford Climatic Chamber" Type PHX73/RR/H/FFF/AUTO/CAM. Temperature measurement shall be by "Comark Electronic Digital Thermometer with an accuracy of \pm 0.1% of reading.

Altitude testing shall be carried out in "Graviner Altitude Chamber", satisfying the requirement of MIL-STO-810C, Method 50 1.1. Proc.I. Pressure levels shall be measured using suitable pressure and vacuum gauges with an accuracy of \pm 2% of reading.

Sand and Oust testing shall be carried out using "Graviner Sand and Dust Chamber", satisfying the requirements of MIL-STD-810C Method 510.1. Proc.I.

Fungus Resistance Tests shall be carried out using "Hedinair Mould Growth Cabinet" satisfying the requirements of British Standard 35.2011, Part J.

Salt, Fog testing shall be carried out using "Graviner Salt Spray Chamber", satisfying the requirements of MIL-STD-810C Method 509.1. Proc.I.

Acceleration testing shall be carried out using "Graseby Centrifuge" Type G.W.3.

Fire Resistance testing shall be carried out using a 6° x 1100° C Torch to Specification TSO C79, **Pigure No.2**.

All pressure and vacuum gauges used shall be calibrated to the requirements of British Standard 85.1780.

All electrical instrumentation used shall be calibrated to the requirements of British Standard $\theta S.89.$

4. Approval Tests

4.1. Examination of Froduct

4.1.1. Weight

The weight of all system components submitted for approval testing shall be checked and recorded.

4.1.2. Size

The dimensions of all system components submitted for approval testing shall be checked to ensure conformity with the relevant drawings.

4.1.3. Visual Examination

All system components submitted for approval testing shall be examined for correctness of marking, workmanship and visible defects.

4.1.4. Centre of Gravity

The centre of gravity for each of the system components shall be established using the "knife edge method".

4.2. Electrical Tests

4.2.1. Voltage Supplies

The system shall operate from nominal 115 volt 400 Hz and 28 volt d.c. power supplies in accordance with MIL-STD-704A, Equipment Category B. Emergency supply conditions.

A.C. Voltage Limits. 102 - 124 volts. 380 - 420Hz

D.C. Voltage Limits. 16 - 29 volts.

System A

C.C.U. 115v, 400Hz and 28v.d.c.

C.W.U. 28v.d.c.

System B

C.C.U. 115v 400Hz

C.W.U. 28v.d.c.

Voltage Transients

The system shall be unaffected by exposure to the following input voltages in accordance with MIL-STD-704A.

Voltage	Duration
190	0.10 second
174	0.40 second
139	4.00 seconds
137	5.00 seconds

After the transient test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3. and the acceptance requirements of the relevant Q. Data Sheet detailed in paragraph 4.4.

Supply Interruption

The effect of voltage supply interruption to the system shall be established.

This test shall be carried out as part of Voltage Transient testing in accordance with MIL-STD-704A.

4.2.2. Insulation Resistance

C.C.U. Using a 30 volt d.c. source, the leakage current between all unearthed terminal pins and case shall not exceed 1.5 µA.

C.W.U. Using a 500 volt d.c. insulation tester the resistance measured between all unearthed connector pins and case shall not be less than 20 Megohms.

Detector Unit
Using a 500 volt d.c. insulation tester
the resistance measured between all unearthed
connector pins and case shall not be less
than 20 Megohms.

4.2.3. Electromagnetic Interference

The complete system shall be tested to comply with the electromagnetic interference requirement of MIL-STD-461.

Testing shall be carried out in accordance with "EMC Test Plan" for Ultra-Violet Advanced Fire Detection System.

4.2.4. Functional Test

4.3. Performance Tests

The following tests, paras. 4.3.2., 4.3.3., and 4.3.4. shall be carried out in accordance with MIL-D-27729A, paras. 3.11.2., 3.11.3., and 3.11.4. modified as follows:

4.3.1. Standard Test Flame

The Standard Test Flame shall be produced by burning JP-4 fuel. or 100 octane gasolene in a 5 inch diameter pan, in an environment in which the airflow does not exceed 10 feet per second.

A U.V. source with the equivalent radiation distribution and intensity may be substituted.

The U.V. source shall satisfy the following requirements :-

When measured at the front face of the detector, irradiance, at wavelength 220nm and bandwidth less than 10 nm, shall not be greater than 3×10^{-10} watts/cm².

Irradiance at any other wavelength between 270 and 320 nm of a bandwidth less than 10nm shall not be greater than 10^{-7} watts/cm².

This satisfies the requirements of a 5° pan fire at a distance of four feet.

4.3.2. Response Time

The system shall respond within 1 second when one Detector Unit is exposed to the Standard Test Flame of para. 4.3.1. at a distance of four feet while simultaneously being exposed to direct unfiltered midday (* 1 hour) sunlight, or its equivalent in U.V. spectral radiation and intensity.

The Detector Units shall be tested independently at the supply voltage extremes detailed in para. 4.2.1.

4.3.3. Reset Time

After having been exposed to the Standard Test Flame of para. 4.3.1. for a period of one minute, the flame shall be cut off from the view of the Detector Unit. The time taken for the warning to clear shall not exceed 1.5 seconds. The Detector Unit shall continuously be exposed to direct sunlight during this test. The test shall be carried out at supply voltage extremes detailed in para. 4.2.1.

4.3.4. Viewing Field

Marie Contraction of the contrac

The Detector Unit shall have a viewing field of at least 80° . This shall be achieved by exposing the Detector Unit to the Standard Test Flame of para. 4.3.1. in the following attitudes and at a distance of four feet.

(a) Detector Unit on a line 40° above the flame centre viewing along a horizontal axis.

- (b) Detector Unit on a line 40° below the flame centre viewing along a horizontal axis.
- (c) Detector Unit on a line 40° to right of flame centre viewing along a horizontal axis.
- (d) Detector Unit on a line 40⁰ to left of flame centre viewing along a horizontal axis.

The system shall meet the response time requirements of para. 4.3.2., and shall be tested at voltage extremes detailed in para. 4.2.1.

4.3.5. False Clearing of Alarm

With the system in a warning condition after having been exposed to the Standard Test Flame of para. 4.3.1., no reset shall occur when 50% of the Test Flame is masked from the view of the Detector Unit. This test shall be carried out at supply voltage extremes detailed in para. 4.2.1.

4.4. Environmental Tests (Sequential)

Environmental tests shall be carried out, where possible, in the following sequence as defined by MIL-STD-810C, paragraph 4, Table I for Group 2 equipment, sequence (a).

Prior to any environmental testing, all squipment shall meet the Acceptance Test Requirements detailed in the following documents :-

Crew Warning Unit - Graviner Q.Oata Sheet No.Q.5305.

Computer Control Unit - Graviner Q.Data Sheet No.Q.

Detector Unit - Graviner Q.Data Sheet No.Q.5304.

These tests shall also be carried out where detailed after environmental tests.

In addition to the above tests, where possible, during the following environmental tests a minimum of three fire response checks shall be carried out in accordance with paragraph 4.3.2.

These checks shall be carried out, shortly after the beginning of the test, at the mid point and just prior to completion.

4.4.1. High Temperature

The component parts of the system shall meet the High Temperature requirements of MIL-STD-810C, Method 501.1, Procedure I, and shall be unaffected by 48 hours at the following temperatures :-

Detector Unit 260°C Computer Control Unit 85°C Crew Warning Unit 71°C

The equipment shall be energised throughout the test. After the test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.2. Low Temperature

The component parts of the system shall meet the Low Temperature requirements of MIL-STD-810C, Method 502.1, Procedure I and shall be unaffected by 24 hours at a temperature of $^{-54}$ C.

After the test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.3. Temperature Shock

The component parts of the system shall meet the Temperature Shock requirements of MIL-STD-810C, Method 503.1, Procedure I, and shall be unaffected by rapid transfer between the following temperatures:

Detector Unit 260°C/-54°C/260°C Computer Control Unit 85°C/-54°C/85°C Crew Warning Unit 71°C/-54°C/71°C

After the test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.4. Altitude

The component parts of the system shall meet the Altitude requirements of MIL-STD-810C, Method 500.1, Procedure I and shall be unaffected by periods of 1 hour each at pressures equivalent to 70,000 feet (1.33 in Hg) and -1000 feet (30.12 in Hg).

After the test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.5. Temperature/Altitude

The component parts of the system shall meet the Temperature/Altitude requirements of MIL-STD-810C Method 504.1, Procedure I, for continuously operating equipment Category 6, and shall be unaffected by exposure to temperatures of -54°C to 71°C with altitudes up to 70,000 feet.

After the test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.6. Sand and Dust

The component parts of the system shall meat the Sand and Dust requirements of MIL-STD-810C, Method 510.1, Procedure I and shall be unaffected by 28 hours exposure to Sand and Dust.

After the test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.7. Humidity

The component parts of the system shall meet the Humidity requirements of MIL-STD-810C, Method 507.1, Procedure I and shall be unaffected by the following test :-

10 cycles of -

- 2 hours to 65°C with 95% RH 6 hours at 65°C with 95% RH 16 hours at 30°C with 85% RH

After the 240 hour test the equipment shall meet the performance requirements of paras. 4.3.2.. 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.8. Fungus Resistance

The component parts of the system shall meet the Eungus Resistance requirements of MIL-STD-810C, Method 508.1, Procedure I. The equipment and suitable control items shall be sprayed with a mixed spore suspension containing the following cultures :-

Aspergillus niger Aspergillus flavus Aspergillus versicolor Pencillium funicolosum Chaetomium gloposum

The test item shall then be stored under cyclic temperature and humidity condition to include 20 hours at 30°C and 95% RH followed by 4 hours at 25°C with 100% RH.

After 7 days the control items shall b. examined and if satisfactory fungus growth is evident the test shall continue for 28 days.

After the test the equipment shall be examined for fungus growth and shall then meet the performance requirements of paras. 4.3.2. 4.3.3 and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.9. Salt Fog

The component parts of the system shall maet the Salt Fog requirements of MIL-STD-810C. Method 509.1, Procedure I and shall be unaffected by 48 hours exposure to a Salt Fog from a 5%, by weight, Sodium Chloride solution.

After exposure, to aid examination, the equipment may be washed in running water, not exceeding $38^{\circ}\mathrm{C}$, and then stored at ambient conditions for 48 hours.

The equipment shall then meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.10. Acceleration

The component parts of the system shall meet the acceleration requirements of MIL-STD-810C, Method 513.2, Procedure I, and shall be unaffected by acceleration levels up to 25.5g.

Acceleration shall be applied in each of three mutually perpendicular planes, in both forward and reverse directions, and shall be held for a minimum of 60 seconds in each direction.

4.4.11. Explosive Atmosphere

Not applicable.

4.4.12. Mechanical Shock

The component parts of the system shall meet the shock requirements of MIL-STD-810C, Method 516.2., Procedure I, and shall be unaffected by shock loads of 20.0g.

The equipment shall be subjected to 18 shock pulses of 20.0g for a duration of 11.0 milliseconds. 3 shocks in each of 3 mutually perpendicular planes in both forward and reverse directions.

After the test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.13. Vibration

The component parts of the system shall meet the vibration requirements of MIL-STD-810C, Method 514.2.

The equipment shall be subjected to the vibration test comprising a Resonance Search, Functional Test and Endurance Test in each of 3 mutually perpendicular axes over the frequency range of 5-2000 Hz.

Resonance Search

The equipment shall be subjected to a sinusoidal resonance search in each of 3 mutually perpendicular exes, over the frequency range of 5-2000 Hz in accordance with MIL-STD-610C, Method 514.2 Procedure I, at the following vibration levels :-

Detector Unit

Figure 514.2-2, Curve G for equipment located in engine compartments.

5-14 Hz 0.10 inch. double amplitude 14-23 Hz 1.0g acceleration

23-90 Hz 0.036 inch. double amplitude

90-2000 Hz 15.0g acceleration.

C.C.U. and C.W.U.

Figure 514.2-2, Curve J for equipment mounted in forward fuselage.

5-14 Hz 0.10 inch. comble amplitude

14-23 Hz 1.0 g acceleration

0.036 inch. double amplitude 23-52 Hz

52-2000 Hz 5.0g acceleration.

Functional and Endurance Test.

The equipment shall be subjected to random vibration in each of 3 mutually perpendicular axes over the frequency range of 15-2000 Hz in accordance with MIL-STD-810C, Method 514.2, Procedure 1A as detailed in Figures 514.2-11A and 514.2-2A at the following vibration levels:

Equipment	Test Levels		
	Maximum P.S.D. g ² /Hz		
	Endurance 1 Hour	Performance 1 Hour	A
C.C.U. and C.W.U.	0.033	0.025	0.02
Detectors	0.33	0.25	0.04

The endurance test may be eliminated if the Functional Test is run for 3 hours.

The equipment shall meet the performance requirements of paras. 4.3.2. and 4.3.3., during the test.

On completion of the vibration test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.14. Acoustic Vibration

The Detector Unit shall meet the Acoustic Vibration requirements of MIL-STD-810C, Method 515.2, Procedure I and shall be unaffected by 30 minutes exposure to a sound pressure level of 150 dB.

After the test the Detector Unit shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of Q.Data Sheet No. Q.5304.

4.5. Environmental Tests (Non Sequential)

4.5.1. Fuel and Oil Immersion

The Detector Unit shall be immersed in JP-4 Fuel, DERC.2454, (MIL-T-5624G) and then allowed to drain for a period of 1 minute. No cleaning shall be accomplished prior to conducting the performance tests of paras.4.3.2. and 4.3.3.

This procedure shall be repeated for the following fluids :-

Turbine 0il DERD 2497 (MIL-L-23699) Hydraulic Fluid DTD 585 (MIL-H-5606)

After the test the Detector Unit shall meet the Acceptance requirements of Q.Data Sheet No.Q.5304.

4.5.2. Rain Spray

The components parts of the system shall meet the Rain Spray requirements of MIL-STD-810C, Method 506.1., Procedure I, and shall be unaffected by a minimum of 30 minutes exposure to rain spray at the rates detailed in the specification.

After the test the equipment shall meet the performance requirements of peras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.5.3. Fire Resistance

Two Detector Units shall be used for this test. One Detector Unit, connector and 6" of wiring shall be immersed in a 6" \times 1100°C flame. The other Detector Unit shall be positioned so as to detect the flame but shall not be immersed in the . flame. The 6" \times 1100°C flame shall be supplied by a burner as detailed in Figure No.2 of MIL-W-25038B. An equivalent burner which may be used for the test is described in Fig. No.2 of Specification TSO.C79.

The Detector Unit shall be immersed in the 6° x 1100°C flame for a period of 5 minutes.

The system shall indicate a fire within 1 second after exposure to the flame and shall continue to indicate for the entire 5 minute exposure.

After the 5 minute period the flame shall be extinguished and the system shall indicate "fire out" within 1.5 seconds.

APPENDIX B-3

- 1. EMI TEST PLAN
- 2. RADIO INTERFERENCE REPORT NO. LM 80876

E.M.I. TESTS FOR ADVANCED AIRCRAFT FIRE DETECTION SYSTEM

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 - 1.1. Testing Aims
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- 2. TEST FACILITY
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 - 2.2. Test Facility for Test Methods 7 and 12
- 3. CALIBRATION OF TEST EQUIPMENT AND ACCURACY OF MEASUREMENTS
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 - 3.2. Accuracy
- 4. OPERATION OF CONTROL UNITS
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 - 4.7. Grounding
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5.0. Chattering relay test

31.3.80 Issue 4

1. FOREWORD

1.1. Testing Aims

The system to be tested consists of one Control Unit type 53813-203, one Control Unit type 53813-204, one Crew Warning Unit type 53813-202, five Dual Detectors type 53522-011, five Single Detectors type 53521-012. The tests to be performed are to demonstrate the system compliance to MIL-STD-461A, NOTICE 3, CLASS A1, and MIL-STD-704A.

1.2. Test Methods

- 1. CEO1 Conducted Emission Power Leads 30 Hz to 20K Hz. (Performed for data purposes only).
- CE02 Conducted Emission Signal and Control Leads 30 Hz to 20K Hz.
- CE03 Conducted Emission Power Leads 100K Hz to 50M Hz.
 (Data to be collected from 14K Hz to 100K Hz for customer information).
- 4. CF04 Conducted Emission Signal and Control Leads 20K Hz to 50M Hz.
- 5. CSO1 Conducted Susceptibility Power Leads 30Hz to 50Hz.
- 6. CS02 Conducted Susceptibility Power Leads 50K Hz to 400M Hz (Note 1)
- 7. CSO6 Conducted Susceptibility SPIKE Power Leads.
- 8. RE02 Radiated Emission Electric Field 14K Hz to 10G Hz.
- 9. RS02 Radiated Susceptibility Magnetic Induction Field (Note 3).
- 10. RS03 Radiated Susceptibility Electric Field 14K Hz to 1G Hz. (Note 2)
- 11. Transient Acceptance to MIL-STD-704A, (Category B).
- 12. Chattering Relay Test (See Section 5).

NOTE 1

Signals 50K Hz - 200 M Hz Modulated on 1 K Hz sine wave (80% modulation). Signals 200 M Hz - 400 M Hz Modulated on 1 K Hz square wave (100% Modulation).

NOTE 2

Signals 50 K Hz - 200 M Hz Modulated on 1 K Hz sine wave (80% modulation). Signals 200 M Hz - 1 G Hz Modulated on 1 K Hz square wave (100% modulation).

NOTE 3

The procedures and limits of method RSO2(a) and (b) shall apply except that the voltage E of part (b) shall be 400 volts across 5 ahms.

1.3. Order of Tests

- a) CE03, b) CE04, c) CE01, d) CE02,
- e) CS01, f) CS02, g) RS03, h) RE02.
- i) Transient acceptance
- k) CS06
- I) RS02
- m) Chattering relay test.

1.4. Test Controls

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All test set ups and techniques are subject to control by MIL-STD-462, Notice 2.

2. TEST FACILITY

2.1. Test Facility for Test Methods 1 to 11

- 2.1.1. Tests will be performed in screened rooms. All power lines entering screened room will be filtered.
- All test equipment will be housed in adjoining screened room for radiated tests. All power lines entering screened room will be filtered.
- 2.1.3. All connections between screened rooms for these tests will be made via coaxial leads and connectors or via an interconnecting screened tube.
- 2.1.4. Coaxial cable insertion loss graphs will be included in the test report where measurements above 100M Hz are recorded.

2.1.5. Ambient Interference Measurements

Prior to each test an ambient calibration for Conducted and Radiated Emission will be performed with the power switches on and the supply line loaded with an impedance equivalent to the system under test.

- 2.1.6. The test facility shall supply a list of what equipment is used in each test.
- 2.1.7. The test facility shall supply detailed descriptions of all test settings and methods according to MIL STD 462 guide lines.

2.2. Test Facility for Test Methods 7 and 12

- 2.2.1. Description of circuit used to produce pulses that are applied to A.C. Aircraft supplies for test method CS06.
 - 2.2.1.1. The equipment used shall consist of a controlled timing current which energises a transient voltage pulse generator having a source impedance of 50 ohm. The pulse is superimposed on the supply so that it coincides with the peak of the 400 Hz waveform either positive or negative going.
- 2.2.2. The test facility shall supply a list of what equipment is used in each test.
- 2.2.3. The test facility shall supply detailed descriptions of all test set ups and methods according to MIL STD 462 guide lines.

3. CALIBRATION OF TEST EQUIPMENT

3.1. Calibration

All equipment used shall be calibrated in accordance with MIL-C-45662 at intervals of six months.

3.2. Accuracy

Frequency When a more accurate measurement than \$\displaystyle 2\% of

the Indicated frequency of the EMI Receiver is

required a frequency counter will be used.

Amplitude Measurements will be within ± 2 dB

of the indicator value.

4. OPERATION OF THE SYSTEM AND OTHER INFORMATION REQUIRED IN PERFORMING THE E.M.C. TESTS

4.1. Operation of the System

4.1.1. Condition 1 STANDBY

This condition is when the UV source is switched off and the "FIRE" and "FIRE DET FAIL" indicators are not illuminated. For CE03 and RE02 a transient condition should be applied by depressing fire test switch periodically during test at a rate of at least 3 operation/resets per octave.

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4.1.2. Condition 2 FIRE

This condition is when the UV source is switched on and the "FIRE" indicators are illuminated on the crew warning unit.

4.1.3. Test Facility

In condition 1 a confidence check can be carried out by depressing the "FIRE DET TEST" switch which illuminates both "FIRE"Indicators, and depressing the "FAIL IND TEST" switch which illuminates the "FIRE DET FAIL" indicators.

4.2. Susceptibility Criteria

The criteria for Susceptibility/Non-Susceptibility will be as follows:-

Condition 1, illumination of any Crew Warning Unit "FIRE" and "FIRE DETECT FAIL" indicators.

Condition 2, cancellation of either "FIRE" indicators.

General, permanent extinction of head emitters when fire test button is depressed.

4.3. Signal and Control Leads to be measured for Conducted Emission

The following leads will be classified as signal and control leads for the Electromagnetic Compatibility Tests:

All leads from Detectors to Control Unit A.

All leads from Detectors to Control Unit B.

Lead from Crew Warning Unit Pin 1 to Control Unit A Pin 34
Lead from Crew Warning Unit Pin 2 to Control Unit A Pin 33
Lead from Crew Warning Unit Pin 9 to Control Unit A Pin 31
Lead from Crew Warning Unit Pin 11 to Control Unit A Pin 30
Lead from Crew Warning Unit Pin 10 to Control Unit B Pin 31
Lead from Crew Warning Unit Pin 12 to Control Unit B Pin 31
Lead from Crew Warning Unit Pin 3 to Control Unit B Pin 34
Lead from Crew Warning Unit Pin 4 to Control Unit B Pin 33
Lead from Control Unit A Pin 35 to Control Unit B Pin 18

The leads will be tested as a bunch. The longest cable to a dual head will be tested. The longest cable to a single head will be tested.

4.4. Power Leads to be Tested:

The following leads will be classified as power leads for the Electromagnetic Compatibility Tests:-

115V 400 Hz.	Line to Control Unit A	Pin 14
115V 400 Hz.	Neutral to Control Unit A	Pin 13
115V 400 Hz.	Line to Control Unit A	Pin 17*
115V 400 Hz.	Neutral to Control Unit A	Pin 16*
115V 400 Hz.	Line to Control Unit B	Pin 14
115V 400 Hz.	Neutral to Control Unit B	Pin 13
28V d.c.	Positive to Control Unit A	Pin 12
28V d.c.	Negative to Control Unit A	Pin 29
28V d.c.	Positive to Control Unit B	Pin 12
28V d.c.	Negative to Control Unit B	Pin 29
28V d.c.	Positive to Crew Warning Unit	Pin 6

^{*} Not to be monitored in CE01, 02, 03, 04 Tests.

4.5. Power Lead Test for Conducted Susceptibility

All live or positives of 4.4 (with the exception of those marked *) to be tested with respect to the relevant neutral or negatives and with respect to earth or by series injection as appropriate.

All neutrals or negatives of 4.4 (with the exception of those marked *) to be tested with respect to earth or by series injection as appropriate.

4.6. Power Lead Connections for Transient Acceptance

For purpose of transient acceptance tests power cables will be linked as follows and treated as a single cable.

1)	115√ 400 Hz.	Line to Control Unit A	Pin 14
·	115V 400 Hz.	Line to Control Unit A	Pin 17
	115∨ 400 Hz.	Line to Control Unit B	Pin 14
	are all linked	together.	

- 2) 115V 400 Hz. NEUTRAL to Control Unit A Pin 13 115V 400 Hz. NEUTRAL to Control Unit A Pin 16 115V 400 Hz. NEUTRAL to Control Unit B Pin 13 are all linked together.
- 3) 28V d.c. POSITIVE to Control Unit A Pin 12 28V d.c. POSITIVE to Control Unit B Pin 12 28V d.c. POSITIVE to crew warning unit Pin 6 are all linked together
- 4) 28V d.c. NEGATIVE to Control Unit A Pin 29 28V d.c. NEGATIVE to Control Unit B Pin 29 are all linked together.

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4.7. Grounding

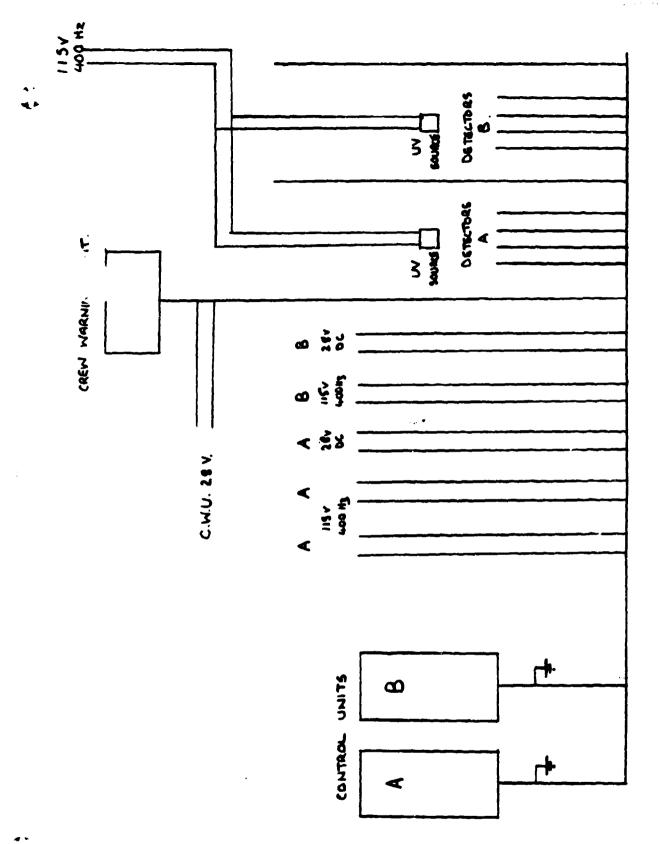
- 4.7.1. The Control Unit and detectors shall be bonded to the Ground plane via short brass straps or brading straps, using dagger pins and retaining screws to simulate aircraft installation.
- 4.7.2. Bonding between the control unit and the ground plane must be equal to or less than 2.5 milliohms DC resistance, and must be recorded as data in the report.
- 4.7.3. The Control Unit Pin 15 will be bonded to the Ground plane via the shortest practical length of wire.
- 4.7.4. The negative lead of the 28V d.c. supply will be bonded to the Ground plane from the screened room wall terminal.

4.8. Lead Length

- 4.8.1. The screened leads from the control unit to the detectors will be 60 ft on one detector and 20 ft on the remaining four detectors for each system.
- 4.8.2. The leads from the control units to the crew warning unit shall be 15 ft.
- 4.8.3. The power leads to the control units will be a nominal 3 ft long for the conducted tests and 6 ft for radiated tests.

5.0. Chattering Relay Test

No change in indications, malfunctions or degradation in performance shall be indicated in any equipment and/or its load when exposed to an impulse type electromagnetic field generated by a type MS 25271 relay (or an acceptable equivalent) when wired for continuous operation with a switch in series with the positive side of the line from a 28V d.c. power source. No suppression components (shielding diode etc.) shall be attached to the relay or its wiring. The unshielded positive lead leaving the switch shall be laid over three sides of the test sample and then connected to the relay. The unshielded return lead from the relay shall be taped to and in parallel with input power leads, signal leads and interconnecting leads. The total length of each external wiring harness parallel with the relay circuit shall not be less than 60". The 28 volt input shall be reversed and the transient repeated.



TEST LAYOUT FIG 1.

Lucas Aerospace Engineering Report

	GRAVINER LTD ADVANCED AIRCRAFT ENGINE
	FIRE DETECTION SYSTEM.

Author. P.P. Curtis	Date 7-7-8 0
Approved by	Date.₩:.३:००
P.D. Campbell	

Lucas Aerospace Electrical Division

Maylands Avenue

Hemel Hempstead

Hertfordshire

Radio Interference Report No. LM 80876

England

3 1 3

Lucas Aerospace

TEST HOUSE CERTIFICATE

Issued Under Defence Quality Assurance Board Approval No. 12870

Civil Aviation Authority Reference D.A.I. 1265/39

Telephone: Hemel Hampstead 42233

Telex: 82110

Lucas Aerospace Limited

Electrical Division Maylands Avenue **Hemel Hempstead** Herrfordshire HP2 4SP

Serial No. H

TO:

GRAVINER LTD POYLE ROAD COLNEROOK SLOUGH SL3 CHB

CONTRACT No.

RELEASE NOTE No.

REQUIREMENTS OF CUSTOMER'S ORDER:

E.M.C. tests to MIL-STD-462 Notice 2 and MIL-STD-461A Notice 3 as detailed in Graviner Test Plan 3.3.80 Issue 4.

DESCRIPTION:

ADVANCED AIRCRAFT FIRE DETECTION SYSTEM.

REPORT: IN 80876

CERTIFICATION:

*Certified that the above mentioned specimens/parts/materials/systems have been tested/exemined in accordance with the terms of the contract/order applicable thereto and unless otherwise stated conform fully to the standards/specifications quoted hereon and the requirements of the Civil Aviation Authority, This does not guarantee the bulk of the items/meternel to be of equal quality.

Date 8-5-80 Signed: . 2 14

For and on behalf of Lucas Aerospace Ltd.



Circulation

GRAVINER 6
A.R. Sharp
File

Summary

The Graviner Advanced Aircraft Fire Detection system was tested to Test Plan 31.3.80 issue 4. The system comprised of two control units types 53813-203 and 53813-204, one Crew Warning Unit type 53813-202, five Dual Detectors type 53522-011 and five Single Detectors type 53521-012.

The tests were performed to demonstrate the system compliance to MIL-STD-461A, Notice 3, Class A1 and MIL-STD-704A.

The equipment complies with the requirements of the following tests:-

- CE.01 30Hz to 20KHz Conducted Emissions Narrowband Power leads.
- CE.02 30Hz to 20KHz Conducted Emissions Narrowband Signal and Control leads.
- CE.03 100KHz to 50MHz Conducted Emissions Broadband and Narrowband Power leads. Condition 1 Standby, and Condition 2 fire.
- RE.02 14KHz to 1GHz Radiated Emissions Broadband Condition 1 Standby.
- RE.02 14KHz to 10GHz Radiated Emissions Narrowband Condition 1 Standby, and Condition 2 fire.
- CS.01 Conducted Susceptibility Power leads 30Hz to 50KHz
- CS.O? Conducted Susceptibility Power leads 50KHz to 400MHz
- RS.03 Radiated Susceptibility 14KHz to 1GHz.

The equipment has emissions outside the specified broadband limits in the following tests:-

CE.03 Fire detect test transients.

The following leads showed transient emissions out of limit caused by the operation of the fire detect test switch on the Crew Warning Unit.

7MHz, 10MHz, 15MHz and 20MHz 115V line Control A pin 14 5MHz, 7MHz, 10MHz, 15MHz and 20MHz 115V Neutral Control A pin 13 28V dc Positive Control A 30KHz, 15KHz and 20MHz . 15MHz and 20MHz 28V dc Negative Control A 5MHz, 7MHz, 10MHz and 15MHz 115V Neutral Control B 7MHz, 10MHz, 15MHz and 20MHz 28V dc Positive Control B 28V dc Negative Control B 20MHz 500KHz, 700KHz, 1MHz, 1.5MHz, 2.0MHz 28V dc Positive C.W.U. 3MHz, 4MHz, 5MHz, 7MHz, 10MHz, 15MHz 20MHz.

CE.04 20KHz to 50MHz Conducted Emissions Signal and Control leads. Condition 1, Standby.

Bunch 1, (All leads, Detectors, Control Units, Crew Warning unit excluding Power supplies). Transient emissions caused by "detector self test check", out of limits between 450KHz and 9.5MHz.

Bunch 2, (Single detector long cable bunch). Emissions out of limit as above between 450KHz and 10.5MHz.

Bunch 3, (Dual detector long cable bunch). Emissions out of limit as above between 650KHz and 4.0MHz.

Condition 2, Fire.

Bunch 1, (All lead, detectors, Control Units, crew warning unit excluding power sup es). Emissions caused by "detection of fire" above the limit between 450kHz and 10MHz.

Bunch 2, (Single Detector long cable bunch). Emissions out of limit as above between 500KHz and 14MHz.

Bunch 3, (Dual Detector long Cable bunch) Emissions out of limit as above between 550KHz and 8MHz.

RE.O2 Radiated Emissions Electric Field 14KHz to 10GHz.

Fire Detect Transients.

The following frequencies show transient emissions out of limit caused by the operation of the fire detect test switch on the Crew Warning Unit.

20KHz, 30KHz, 45KHz, 65KHz,80KHz, 100KHz, 150KHz, 200KHz, 1MHz, 3MHz, 4MHz, 10MHz, 40MHz and 150MHz.

Condition 2 Fire.

The radiated emissions were marginally above the limit between 14KHz and 20KHz and 5.75MHz and 6.5MHz.

The transient voltage and spike tests undertaken at Lucas Aerospace Ltd., Bradford are detailed in a separate report included within this report. See appendix No. 5.

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E.M.C. Test CE.02

E.M.C. Test RE.02

E.M.C. Test C8.01

E.H.C. Tost CS.02

E.M.C. Test RS.03

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Appendix 1 Test Layouts

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Ampendix 3 Test sample circuit modifications

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Appendix 5 Tests undertaken at Bradford Report No. AED/ENV/480550

Introduction

This report details E.M.C. tests carried out on the Graviner Ltd., Advanced Aircraft Engine Fire Detection System. The tests described herein were carried out in accordance with the Graviner Ltd., Test Plan No. 31-3-80 issue 4.

The tests described in this report were carried out at Lucas Aerospace facilities at Hemel Hempstead and Bradford.

Equipment Under Test

Ultra Violet Advanced Fire Detection Control Unit Pt. No. 53813-203 Serial No. 100.

Ultra Violet Advanced Fire Detection Control Unit Pt. No. 53813-204 Serial No. 100.

Crew Warning Unit Pt. No. 53813-202 Serial No. 100. 5 off Single Detector Units Pt. No. 53521-012. 5 off Dual Detector Units Pt. No. 53522-011.

Associated Equipment.

Aircraft cable form

Neon lights

Gnd test box.

Fibre optic cables for system warning lamps.

Test Equipment

Stoddart 91550-1 current probe Ser. No. 421/130
Stoddart 91197-1 current probe Ser. No. 218
Electro-Metrics CIG.25 impulse generator
Fairchild PCL-10 current probe + PCL10A amplifier Ser. No. 471
Electro-Metrics Antenna Selector SU125 Ser. No. 143
Fairchild RVR 25 Rod antenna and coupler Ser. No. 6-23
Fairchild BIA 25 Biconical antenna Ser. No. 6-23

Test Equipment (Cont'd)

Stoddart 93490-1 Conical log-spiral antenna.

EMCO 3103 Conical log-spiral antenna Ser. No. 2127

EMCO 3105 Double Ridged Guide Antenna Ser. No. 2091

Electro-Metrics Log periodic antnna LA-70

Lucas manufactured mono-conical antenna

I.F.I. EFG 2 broadband antenna Ser. No. 34

Solar 6552 audio amplifior

Solar 62201A audio transformer

Solar 6512 10uF Feedthrough capacitors 9 off

Dubillier SBC 45 10uF feedthrough cpacitors 2 off

Marconi V.T.V.M. TF 2604 Ser. No. 200933/037

Marconi T.F.200 Signal Generator Ser. No. 54706/14

Marconi T.F. 144H4 Signal Generator Ser. No. 53698/12

Marconi T.F. 801D/1 Signal Generator Ser. No. 53599/24

Marconi V.T.V.M. TF1041B Ser. No. JA217/484

Fairchild EMC10E Measuring Set Ser. No. 10471E

Electro-Metrics EMC25 MK III Measuring Set Ser. No. 366

Stoddart NM65T Measuring Set Ser. No. 145.

Electro-Metrics Programmer ESC 125A Ser. No. 146

Electro-Metrics X-Y plotter 1258 Ser. No. 003

I.F.I. LPA Levelling pre-amplifier Ser. No. 0374942.

I.F.I. EFS1 E-Field Sensor 2 off

I.F.I. LMT Light Modulator/Transmitter 2 off

Bird 8135 termaline co-axial resistor Ser. No. 6829

Radial AdB pad 15 watt.

I.F.I. Wideband amplifier Ser. No. 0374936

Coupling capacitors Lucas 1.0uF, 0.1uF and 0.01uF

2 off fibre optic cables

AML C203 power signal generator Ser. No. 125

AML 7050H plug-in-head 200-450MHz Ser. No. 119

AML 7051 AH plug-in-head 450-750MHz Ser. No. 104

AML 7051BH plur-in-head 750-1GHz Ser. No. 105.

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Report No. LM 80876

Lucas high pass filter (400Hz isolation) Lucas 25uH choke.

Texacan filters:- MCD 6LE 330AB Ser. No. 2888-1

MOD 6LE 494AB Ser. No. 2889-1

MOD SLE 741AB Ser. No. 2890-1

MOD 6LD 1111AB Ser. No. 2891-1

Solar 7021-1 phase Shift network Solartron 1484 True RMS voltmeter Ser. No. 137366

E.M.C. Tests General

The tests were carried out in a screened enclosure as described in the test plan. Interconnection cable assemblies simulated the actual installation and use. Leads that are screened in the normal installation were screened in the test installation. As far as possible, cables and equipments were arranged so that no shielding was interposed between the test sample, cables, and measuring antennas. All leads and cables were within 10 ± 2 cm of the edge of the ground plane and approximately 5 cm above the ground plane. Grounding of the system units was accomplished by copper braid attached to a single ground point. All the ground straps had an impedance of between 0.75 mohms and 1 mohm.

The test sample layouts are shown in ampendix 1.

Screened Room Supplies

The 115V a.c. 400Hz Supplies and the 28V d.c. Supplies were brought into the screened room via filters located within the screened room walls,

E.H.C. Test CE.03

Conducted emissions Power leads 10KHz to 50MHz.

Test equipment.

- a) Current probes Stoddart 91550-1 and 91197-1
- b) Electro-Metrics EMC25 MK.III measuring set Ser. No. 366
- c) Ten microfarad capacitors.
- d) Electro-Metrics Programmer ESC 25A.

Test Schedule.

The E.M.C. test was conducted in accordance with the requirements of MIL-STD-461A Notice 3 and MIL-STD-462 Notice 2, test CE.03. Input power supplies to the test items were connected via 10uF feedthrough capacitors bonded to the ground plane. There was a minimum separation between cables, leads and the ground plane of 5 cm. The length of each power lead between the test sample and the 10uF capacitor was a minimum of one metre. The arrangements for the test are illustrated in appendix 1 Fig. No. 1. The power leads which were separately measured for conducted emissions were as follows:-

115V 400Hz Line to Control Unit A Pin 14
115V 400Hz Neutral to Control Unit A Pin 13
28V d.c. Positive to Control Unit A Pin 12
28V d.c. Negative to Control Unit A Pin 29
115V 400Hz Line to Control Unit B Pin 14
115V 400Hz Neutral to Control Unit B Pin 13
28V d.c. Positive to Control Unit B Pin 12
28V d.c. Negative to Control Unit B Pin 29
28V d.c. Positive to Control Unit B Pin 29

Each lead was subjected to 3 modes of test as follows:-

Condition 1. STANDBY.

Where the U.V. source is switched off and the "FIRE" and "FIRE DET FAIL" indicators were not illuminated.

Condition 1 (a).

Test samples were set as for STANDBY. A Transient condition was applied by depressing the fire test switch periodically at a rate of approximately 3 operation/resets per octave.

Condition 2 FIRE.

Where the U.V. source was switched on and the "FIRE" indicators were illuminated on the crew warning unit.

Test Results

The test results are contained in appendix 2, the appendix contains X-Y plot data of the conducted emissions on each power line listed in the schedule. Page nos. 1 to 9 inclusive appendix 2 detail the conducted emissions when the system was operated in conditions 1 and 1 (a).

At no frequency are there emission above the limit when the system is operated in Standby, condition 1.

When the system was operated in condition 1(a) the following above limit emissions were recorded.

Ľ	EAD	X-Y	PAGE NO.	Frequency	db above limit
115V L	ine Contr	ol A	1	5.OMMz	0.5
**	11	A	1	7.OMHz	5.0
**	17 17	A	1	10.0MHz	3.5
**	17 11	A	1	15.0MHz	3.0
**	11	A	1	20.0MHz	1.0
115V N	eutral Co	ntrol A	2	5.0MHz	1.5
17	**	*1	2	7.0MHz	8.5
**	11 11	••	2	10.0MHz	9.0
**	11	**	2	15.0MHz	8.5
**	17	**	2	20.0MH2	4.0
28V d.	c. Positi	ve Control A	3 .	30.0KHz	0.5
11	11	**	3	85.0KHz	0.5
er e	• • • • • • • • • • • • • • • • • • • •	**	3	15.0MHz	4.0
77 1	••	**	3	ZO.OMEz	6.5
28V dc	Negative	Control A	4	15.0M2	5.0
••	17	**	4	20.0MHz	10.0
115V N	outral Co	ntrol B	6	7.0MHz	10.0
97	11 11	**	6	10.0MHz	12.0
11 1	••	**	6	15.0MHz	12.0
28V dc	Positive	Control B	7	7.OMHz	1.0
11 1	11	**	7	10.0MH2	0.5
**	• "	• ••	7	15.0MH2	8.0
10	" "	••	7	20.0MHz	5.0
28V dc	Negative	Control B	8	20.0MHz	2.0
28V dc	Positive	C.W.U.	9	500KH2	4.0
**	• •	**	9	700KHz	1.5
ff (• •	**	9	1.OMHz	7.0
11 (**	**	9	1.5MHz	5.0
11 (••	9	2.0MHz	9.0
**	• • • • • • • • • • • • • • • • • • • •	**	9	3.OffHz	2.0
**	• • • • • • • • • • • • • • • • • • • •	"	9	4.ONHz	5.0
" 1	1 11	"	9	5.0MHz	5.0
77	• •	**	9	7.0MHz	4.0
**	, ,,	**	9 3/4	10.0MRz	14.0
**	* **	**	9	15.0MHz	5.0
" (, ,,	10	1	20MI2	5,0

Page Nos. 10 to 18 inclusive app. 2 detail the power lead conducted emissions when the system is operated in condition 2 "FIRE".

The X-Y plots show that there are no emissions above the limit.

Throughout all modes of system operation there were no narrowband emissions and therefore the system meets the narrowband requirements.

11.17

EMC Test CE.04

Conducted emissions Signal and Control leads 20KHz to 50MHz.

Test equipment.

- a) Current probes Stoddart 91550-1 and 91197-1
- b) Electro-Hetrics EMC-25 MK.III measuring set Ser. No. 366
- c) Ten microFarad capacitors
- d) Electro-Metrics programmer ESC 25A.

Test Schedule.

The E.N.C. test was conducted in accordance with the requirements of MIL-STD-461A Notice 3 and MIL-STD-462 Notice 2, test CE.04 Input power supplies to the test items were connected via 10uF feedthrough capacitors bonded to the ground plane. There was a minimum separation between cables, leads and the ground plane of 5 cm. The length of each power lead between the test sample and the 10uF capacitor was a minimum of one metre. The arrangements for the test are illustrated in appendix 1 Fig. No. 1. The control and signal lead bunches were separately measured for conducted emissions as follows:-

Bunch 1, All leads, Detectors, Control Units, Crew Warning Unit, excluding power supplies.

Bunch 2. Single detector long cable bunch.

Bunch 3. Dual detector long cable bunch.

Each bunch was subjected to 2 modes of test as follows:-

Condition 1 STANDBY.

Where the U.V. source is switched off and the "FIRE" and "FIRE DET. FAIL" indicators were not illuminated.

Condition 2 FIRE.

Where the U.V. source was switched on and the "FIRE" indicators were illuminated on the crew warning unit.

Test Results.

The test results are contained in appendix 2, the appendix contains X-Y plot data of the conducted emissions on each bunch listed in the schedule. Page nos. 19 to 21 app. 2 inclusive detail the conducted emissions when the system was operated in condition 1, Standby.

The X-Y plot on page 19 app. 2. Bunch 1, shows transient emissions above the limit between 450KHz and 9.5MHz. The maximum emission above the limit is 25dB between 2.3 and 2.4MHz.

Page 20 spp. 2, Bunch 2, shows transient emissions above the limit between 450KHz and 11.75MHz. The maximum emission above the limit is 22dB between 2.3 and 2.4MHz.

Page 21 app. 2, Bunch 3, shows transient emissions above the limit between 600KHz and 800KHz, and between 1.2MHz and 4MHz. The maximum emission above the limit is 25dB between 2.3 and 2.4MHz.

Page nos. 22 to 24 app. 2. inclusive detail the conducted emissions when the system is operated in condition 2, Fire.

The X-Y plot on page 22, app.2, Bunch 1, shows emissions above the limit between 450KHz and 10MHz. The maximum emission above the limit is 27dB between 2MHz and 2.2MHz.

The X-Y plot on page 23, app.2, Bunch 2, shows emissions above the 'imit between 480KHz and 610KHz, and between 850KHz and 13MHz. The maximum emission above the limit is 20.5 dB between 2.05MHz and 2.3MHz.

The X-Y plot on page 24, anp. 2, Bunch 3, shows emissions above the limit between 580KHz and 670KHz, between 1 MHz and 5MHz, at 6.6MHz and at 7.8MHz. The maximum emission occurs at 2.1MHz and is 28.5dB above the limit.

Throughout the two modes of system operation there were no narrowband emissions and therefore the system meets the narrowband requirements.

E.M.C. Test CE.01

Conducted emissions Power leads 30Hz to 20KHz.

Test Equipment.

- a) Current Probe PCL-10
- b) PCL 10A Amplifier for use with (a).
- c) Electromagnetic Interference Meter Fairchild EMC10E
- d) 10uF feedthrough capacitors
- e) Electro-Metrics Programmer ESC 25A.

Test Schedule.

The E.M.C. test was conducted in accordance with the requirements of MIL-STD-461A Notice 3 and MIL-STD-462 Notice 2 test CE.01. Input power supplies were connected to the test items via 10uF feedthrough capacitors bonded to the ground plane. There was a minimum separation between leads, cables and the ground plane of 5cm. The length of each power supply lead between test sample and the 10uF capacitor was a minimum of one metre. The arrangements for the test are illustrated in appendix 1, fig. No. 1. The power supply leads which were separately measured for conducted emissions were as follows:-

115V 400Hz line to Control Unit A Pin 14
115V 400Hz Neutral to Control Unit A Pin 13
28V dc Positive to Control Unit A Pin 12
28V dc Negative to Control Unit A Pin 29
115V 400Hz Line to Control Unit B Pin 14
115V 400Hz Neutral to Control Unit B Pin 13
28V dc Positive to Control Unit B Pin 12
28V dc Negative to Control Unit B Pin 29
28V dc Positive to Crew Warning Unit Pin 6.

Each lead was subjected to 2 modes of test as follows:-

Condition 1 STANDBY.

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Where the U.V. source is switched off and the "Fire" and "Fire Det. Fail" indicators were not illuminated.

Condition 2 FIRE.

Where the U.V. source was switched on and the "FIRE" indicators were illuminated on the crew warning unit.

Test Results.

The test Results are contained in appendix 2, the appendix contains X-Y plot data of the conducted emissions on each power line listed in the schedule. Page nos. 25 to 33 app. 2 inclusive detail the conducted emissions when the system was operated in Condition 1. At no frequency were there narrowband emissions above the limit when the system was operated in Condition 1, STANDBY.

Page nos. 34 to 42 inclusive appendix 2 detail the power lead conducted emissions above the limit when the system was operated in condition 2 "FIRE". The X-Y plots show that there are no narrowband emissions above the limit.

E.M.C. Test CE.OZ

Conducted emissions signal and control leads 30Hz to 20KHz.

Test equipment.

- a) Current Probe PCL-10
- b) PCL 10A Amplifier for use with (a)
- c) Electromagnetic Interference Meter Fairchild EMC10E
- d) Electro-metrics Programmer ESC 25A.

Test Schedule.

The E.M.C. test was conducted in accordance with the requirements of MIL-STD-461A Notice 3 and MIL-STD-462 Notice 2, test CE.O2. Input power supplies were connected to the test items via 10uF feedthrough capacitors bonded to the ground plane. There was a minimum separation between cables, leads and the ground plane of 5cm. The length of each power lead between the test sample and the 10uF capacitor was a minimum of one metre. The arrangements for the test are illustrated in appendix 1. Fig. No. 1. The control and signal lead bunches were separately measured for conducted emissions as follows:-

Bunch 1, All leads, Detectors, Control Units, Crew Warning Unit, excluding power supplies.

Bunch 2. Single Detector long cable bunch.

Bunch 3. Dual Detector long cable bunch.

Each bunch was subjected to two modes of test as follows:-

Condition 1. STANDBY.

Where the U.V. source was switched off and the "FIRE" and "FIRE DET. FAIL" indicators we'. not illuminated.

Condition 2. FIRE.

Where the U.V. source was switched on and the "FIRE" indicators were illuminated on the crew warning unit.

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Test Results.

The test results are contained in appendix 2, the appendix contains X-Y plot data of the conducted emissions on each bunch listed in the schedule. Page nos. 43 to 45 app. 2. inclusive detail the conducted emissions when the system was operated in condition 1 Standby. Page nos. 46 to 48 app. 2 inclusive detail the conducted emissions when the system was operated in condition 2 Fire. No X-Y plot shows narrowband emissions above the limit.

E.M.C. TEST RE.OZ

Radiated Emission 14KHz to 10GHz Electric Field.

Test equipment.

- a) Test antennas 41" Rod, Bi-conical, Conical Log Antenna, Double ridged guide Antenna.
- b) E.M.I. meters EMC 25 and NM65T
- c) Electro-metrics programmer ESC25A
- d) 10uF feedthrough capacitors.

Test Schedule.

The E.M.C. test was conducted in accordance with the requirements of MIL-STD-461A Notice 3 and MIL-STD-462 Notice 2, test RE.02. Input power supplies to the test items were connected via 10uF feedthrough capacitors bonded to the ground plane.

There was a minimum separation between cables, leads and the ground plane of 5cm. The length of each power lead between the test sample and the 10uF capacitor was a minimum of two metres. The arrangements for the test are illustrated in appendix 1. Fig. nos. 2, 3, 4 and 5. The system was tested in three modes as follows:-

Condition 1. STANDBY.

Where the U.V. source has switched off and the "FIRE" and "FIRE DET. FAIL" indicators were not illuminated.

Condition 1(a).

Test samples were set up as for STANDBY. A Transient condition was applied by depressing the fire test switch periodically at a rate of approximately 3 operation/resets per octave.

Condition 2. FIRE.

Where the U.V. source was switched on and the "FIRE" indicators were illuminated on the crew warning unit.

Test Results

The test results are contained in appendix 2, the appendix contains X-Y plot data of emissions in all three modes of operation.

Page 49 and 50 show the radiated broadband emissions from 14KHz to 1GHz when the system was operated in modes 1 and 1 (a).

In mode 1, Standby the only emissions above the limit occur at 15KHz and 16KHz where the levels are both 0.5 dB above the limit. There were no narrowband emissions exhibited on the X-Y plot.

In mode 1(a) the following above limit transient emissions were recorded.

X-Y PAGE NO.	FREQUEICY	db above limit
49	14KHz	3
49	20KHz	12.5
49	30KHz	13
49	45KHz	14.5
49	65KHz	15
49	80KHz	12
49	100KHz	9•5
49	150KHz	2.5
49	2001Hz	8.5
49	1MHz	1,5
49	3MHz	6
49	4MHz	7
49	10/4Hz	5
49	40MHz	2
50	150MHz	2

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Graph nos. 51 and 52 show the narrowband X-Y plot 1-10GHz for when the system was operated in "Standby". There are no narrowband emissions. The emissions above the limit shown on band 1 are broadband.

The X-Y plots on pages 53 and 54 show the radiated broadband emissions from 14KHz to 1GHz, when the system was operated in mode 2 "Fire".

The radiated emissions above the limits occur at between 14KHz and 18KHz, and 5.75MHz and 6.6MHz. The maximum emission occurred at 6.4MHz, where the level was 6dB above the limit. There were no narrowband emissions exhibited on the X-Y plot. Graph nos. 55 and 56 show narrowband X-Y plot 1-10GHz for when the system was operated in "Fire". There were no narrowband emissions. The emissions above the limit shown on band 1 are broadband.

E.M.C. Test CS.01

Conducted Susceptibility, 30Hz to 50KHz. Power leads.

Test equipment.

- a) Oscillator Marconi TF 2000 & TF144/H4
- b) Power Amplifier Solar 6552-1
- c) Isolation Transformer Solar 6220-1A
- d) 400uF capacitor
- e) Marconi V.T.V.M. TF1941B
- f) Solar Phase Shift network.

Test Schedule.

The E.M.C. test was conducted in accordance with the requirements of MIL-STD-461A Notice 3 and MIL-STD-462 Notice 2, test CS.01. Input power supplies were connected to the test items via a 10uF feedthrough capacitor bonded to the ground plane. The arrangement for the test is shown in fig. 6. appendix 1. The system was tested in two modes of operation as follows:-

Condition 1. STANDBY.

Condition 2. FIRE.

Test Results

When the initial test results were undertaken it was found that when any d.c. lead of the system was tested in condition 1, STANDBY there were malfunctions. The malfunctions were identified by either or both the Fire warning lights illuminating. The susceptibility occurred between 3.5KHz and 50KHz.

After investigation, (buth CS.01 and CS.02 test methods), the following modifications were made to the system.

- 1) The screen of the detector leads was in each case grounded at the control units and not as originally at the detectors.
- 2) The common logic cards power supply input filters in both control units were modified by including two 6.8uF capacitors between the 28V d.c. positive and negative leads to ground. See figure 1., appendix 3.
- The drive supply cards, (two in control unit A and one in control unit B), were modified by decoupling the 10Kohm resistors R25, R27, R29, R31, R49, R51, R53, and R55 with 10,000 p.F. capacitors. See figure 2, appendix 3.

Note: After the susceptibility tests were completed the emission tests were repeated and where necessary the X-Y plots were re-plotted. The emission results given in this report are the final levels obtained after the above modifications had been engineered into the system.

With the system modified as detailed above there were no malfunctions throughout test CS.01 on any lead in either of the two modes.

E.M.C. Test CS.02

Conducted Susceptibility 50KHz to 400MHz. Power leads.

Test equipment.

- a) Marconi VTVM TF 1041B
- b) Marconi VTVM TF 2604
- c) Solar 6512 10uF feedthrough capacitors.
- d) Marconi Signal Generator TF 144H/4
- e) Marconi Signal Generator TF 801D/1
- f) IFI LPA1 Levvelling pre-amplifier
- g) Radiall 6dB pads
- h) Marconi 50 ohm load TM5582
- i) Lucas coupling capacitors 1.0uF, 0.1uF, and 0.01uF
- j) Lucas high pass filter (400Hz isolation)
- k) IFI Wideband amplifier
- A.M.L. C203 power signal generator
- m) A.M.L. 7050H plug in head 200-450MHz
- n) 25uH choke (frequency limit 1MHz)
- o) Texacan Filters

Test Schedule.

The E.M.C. test was conducted in accordance with the requirements of MIL-STD-461A Notice 3 and MIL-STD-462 Notice 2, test CS.02. Input power supplies were connected to the test items via a 10uF feedthrough capacitor bonded to the ground plane. The arrangements for the test are shown in fig. ? appendix 1. The system was tested in two modes as follows:

Report No. LM 80876

Condition 1. Standby.

Condition 2. Fire.

Note the susceptibility signal was modulated to Graviner Test Plan 3.3.80 issue 4 requirements.

Test Results.

After the modifications detailed in the CS.01 test were incorporated in the system there were no malfunctions throughout the CS.02 test, on any lead in either mode.

E.M.C. Test RS.03

Radiated Susceptibility 14KHz to 1GHz Electric Field.

Test equipment.

- a) I.F.I. LPA 1 Levelling pre-amplifier
- b) EFS.1 E-field sensors 2 off
- c) IFI Light Modulator/Transmitter
- d) Bird Termaline co-axial resistor.
- e) IFI Wideband amplifier
- f) Fibre optic cables
- g) A.M.L. C203 power signal generator
- h) A.M.L. Plug in heads 7050H, 7051AH, 7051BH 200MHz-1GHz
- i) EMCO 3103 Con. Log. spiral antenna 100-1000MHz
- j) IFI Broadland antenna 10KHz-2001Hz
- k) Marconi Signal Generators TF144/H, TF801/D
- 1) Stoddart Con. Log spiral antenna 93490-1
- m) Stoddart Con. Log spiral antenna 93491-2
- n) EMC 25 measuring set
- o) Texscan Filters MOD 6LE 330AB, MOD 6LE 494B, MOD 6LE 741AB and MOD 6LD 1111AB

Test Schedule.

The E.M.C. test was conducted in accordance with the requirements of MIL-STD-461A Notice 3 and MIL-STD-462, Notice 2, test RS.O3. Input power supplies were connected to the test; via a 10uF feedthrough capacitor bonded to the ground plane. The second state of the test are shown in figs. 8, 9 and 10 appendix 1. The second state of the test are follows:-

Report No. LM 80876

Condition 1. Standby

Condition 2. Fire.

Note the susceptibility signal was modulated to Graviner Test Plan 3.3.80 issue 4 requirements.

Test results.

In condition 1, Standby there were several susceptibilities to the general E-field as follows:-

Frequency	Threshol		Malfunction					
118M2	7 v/m	Righ	t Eng.	. Fire	det.	fail	lamp	illuminated.
121.5MHz	10 v/m	••	**	11	17	**	19	**
124MHz	10 v/m	••	**	**	10	**	**	11
193MHz	8.5 v/m	Left	Eng.	Fire	det.	fail	lamp	illuminated.
200MHz	10 v/m	**	**	10	**	**	**	n

At no frequencies were there malfunctions of the system when the specified E-field level was transmitted.

There was no susceptibility to the radiated E-field when the system was tested in condition 2 fire.

Conclusions

With the system modified as described in the report text, see figs. 1 and 2 appendix 3, the following test results were noted.

E.M.C. Test CE.03

There were no narrowband emissions detected during the test in the two modes of operation therefore the system complies with the CE.03 narrowband requirements. There were no broadband emissions above the limit when the system was operated in condition 1, STANDBY.

In condition 1(a) where transient emissions were recorded when the fire test switch was depressed and reset, there were many emissions above the broadband limits. The table in the CE.O3 results details all the leads and frequencies when the transient emissions were above the limit. The major emissions above the limit are as follows:-

LEAD			X-Y PAGE NO.	FREQUENCY	AB ABOVE LIMIT
115V Neut	ral Control	LA	2	7.OMHz	8.5
71 11	11	19	2	10.0Mtz	9.0
" "	11	**	2	15.0MH2	8.5
28V dc Po	sitive Cont	rol A	3	20.0MHz	6.5
28V de ile	gative Cont	rol A	4	20.0MHz	10.0
115V Neut	ral Control	В	6	7.OMHz	10.0
** "	11	**	6	10.0Mz	12.0
11 11	"	**	6	15.0MHz	12.0
28V de Po	sitive Cont	rol B	7	15.0MHz	8.0
28V dc Po	sitive C.W.	.U.	9	1.OMHz	7.0
11 11	**	**	9	2.OMiz	9.0
11 11	#1	**	9	10.0MHz	14.0

Although the above table details emissions which are significantly above the limit, as they are of a transient nature and the repetition rate low they would not in the opnion of the Lucas Aerospace E.M.C. personnel cause a serious E.M.C. hazard.

In condition 2, Fire, there were no broadband emissions above the limit on any lead.

E.M.C. Test CE.04.

There were no narrowband emissions detected during the test in the two modes of operation therefore the system complies with the CE.O's narrowband requirements.

There were broadband emissions above the limit when the system was tested in condition 1, Standby as follows. Bunch 1, all leads, detectors, control units, and crew warning unit, excluding the power supplies, had emissions above the limit between 450KHz and 9.5MHz. The maximum emission occurred at between 2.3 and 2.4MHz and was 25dB above the limit.

Bunch 2, single detector long cable bunch, had broadband emissions above the limit between 450KHz and 11.75MHz. The maximum emission above the limit is 22 dB between 2.3 and 2.4MHz.

Bunch 3, dual detector long cable bunch, had broadband emissions above the limit between 600KHz and 800MHz and 1.2NHz and 4MHz. The maximum emission above the limit was 25dB between 2.3 and 2.4MHz.

There were also broadband emissions above the limit when the system was operated in condition 2, Fire, as follows.

Bunch 1, all leads, detectors, control units, and crew warning unit, excluding power supplies had emissions above the limit between 450KHz and 10MHz. The maximum emission above the limit is 27dB between 2MHz and 2.2MHz.

Bunch 2, single detector long cable bunch, had emissions above the limit between $480 \mathrm{KHz}$ and $610 \mathrm{KHz}$, and $850 \mathrm{KHz}$ and $13 \mathrm{MHz}$. The maximum emission above the limit is $20.5 \mathrm{dB}$ between $2.05 \mathrm{MHz}$ and $2.3 \mathrm{MHz}$.

Bunch 3, dual detector long cable bunch, had emissions above the limit between 580KHz and 670KHz, 1MHz and 5MHz, and 6.6MHz and 7.8MHz. The maximum emission occurs at 2.1 MHz and is 28.5dB above the limit.

All the above out of specification broadband emissions could be a source of E.M.C. hazard if the aircraft cable layout enabled close coupling to occur between the Fire detect system wiring and leads to other systems. However from the RE.O? test results detailed in this report it would appear that the out of limit emissions are centained within the system wiring as there were no radiated emissions recorded above the limits at the above frequencies.

E.M.C. Test CE.01.

There were no narrowband emissions outside the limits recorded from any of the leads under test in either of the two modes of system operation.

E.M.C. Test CE.02.

There were no narrowband emissions outside the limits recorded from any of the bunches under test in either of the two modes of system operation.

E.M.C. Test RE.02.

There were no narrowband emissions detected during the test in the two modes of operation therefore the system complies with the RE.O2 narrowband requirements.

In condition 1, Standby, there were broadband emissions marginally outside the specification limits between 14KHz and 16KHz. The maximum emission being only 0.5dB above the limit. When the system is operated in condition 1(a) transient emissions above the limit were recorded when the fire test switch was depressed and reset. The table in the RE.02 results details all out of limit transient emissions. The major emissions recorded above the limit are as follows.

X-Y PAGE NO.	FREQUENCY	dB ABOVE LINIO
49	20KHz	12.5
49	30KHz	13
49	45KHz	. 14.5
49	65KH z	15
49	80KHz	12
49	100KHz	9•5
49	200KHz	8.5
49	3MHz	6
49	4MHz	?

Although the above table details emissions which are significantly above the limit, as they are of transient nature and the repetition rate low, they would not in the opinion of the Lucas Aerospace E.M.C. personnel cause a serious E.M.C. hazard.

In condition 2, Fire, there were broadband emissions above the limit between 14KHz and 18KHz, between 5.75MHz and 6.6MHz. The maximum emission occurred are 6.4MHz where the level was 6dB above the limit. It is considered by the Lucas Aerospace E.M.C. personnel that these radiated emissions would not cause an E.M.C. hazard in the aircraft installation.

E.M.C. Test CS.01.

The test was performed with the circuit and cable modifications as described earlier. There were no susceptibilities throughout the test on any lead in either of the two conditions of system operation.

E.M.C. Test CS.02.

The test was performed with the circuit and cable modifications as described earlier there were no suscentibilities throughout the test on any lead in either condition of system operation.

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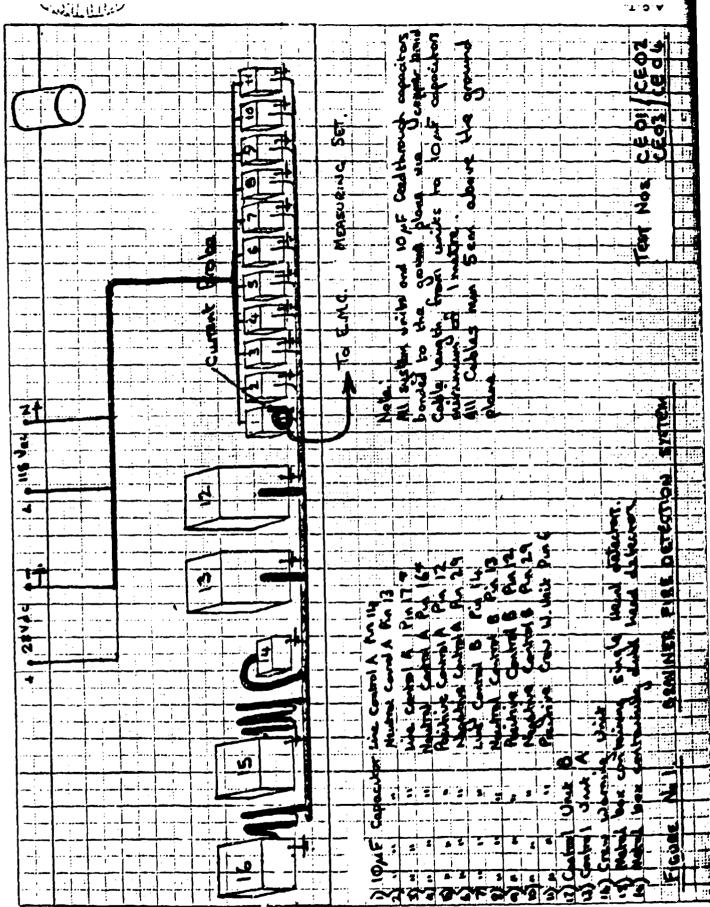
E.M.C. Test RS.03.

In condition 1, Standby, there were several frequencies as detailed in the report where the system malfunctioned, i.e. Eng. Fire detect lamps illuminated. At no frequency were there malfunctions of the system when the specified E-field level was transmitted.

The results contained in this report only apply to equipment manufactured to the same standards as that submitted for testing any deviation from these standards could invalidate these results.

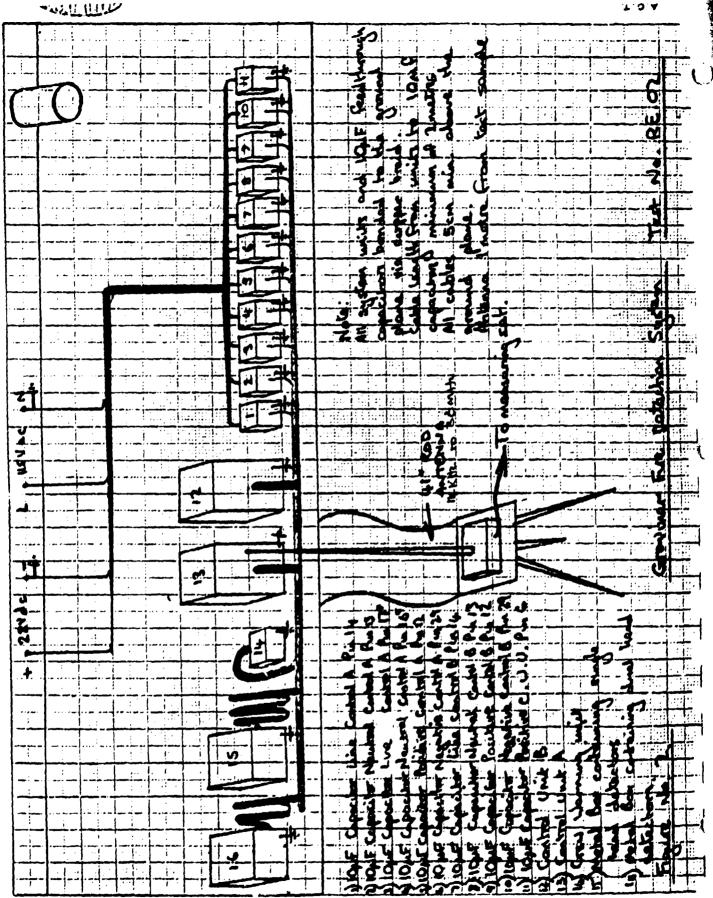
Appendix 1

Test Layouts

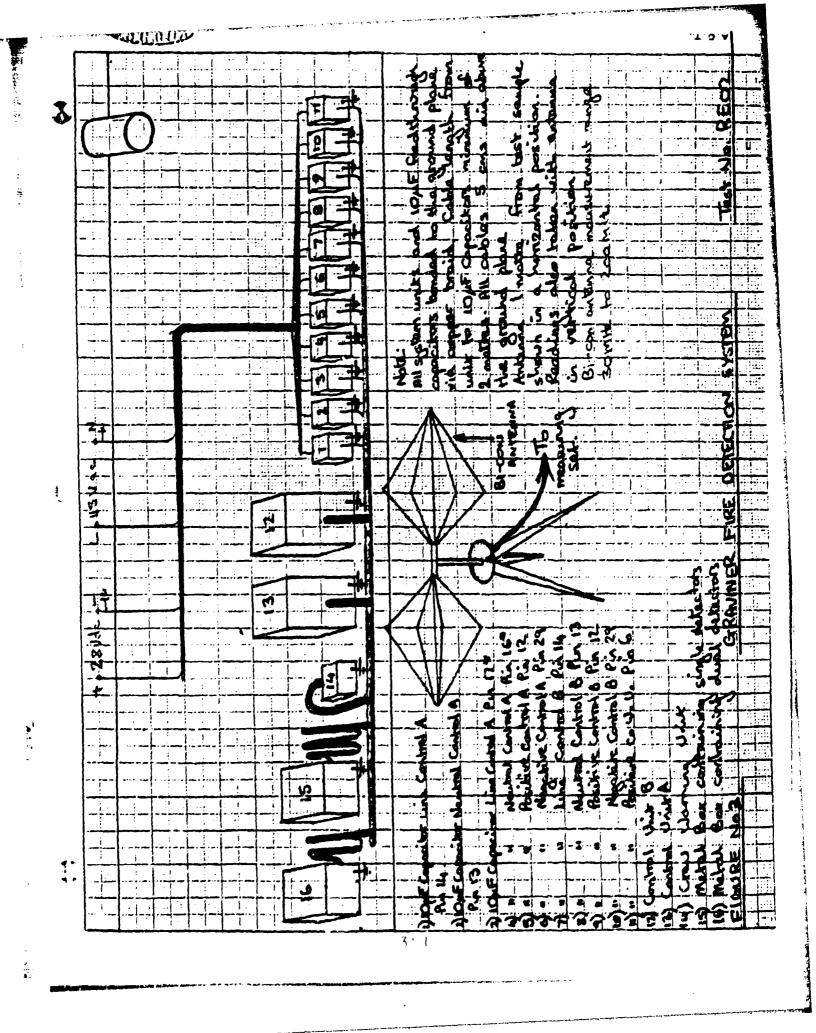


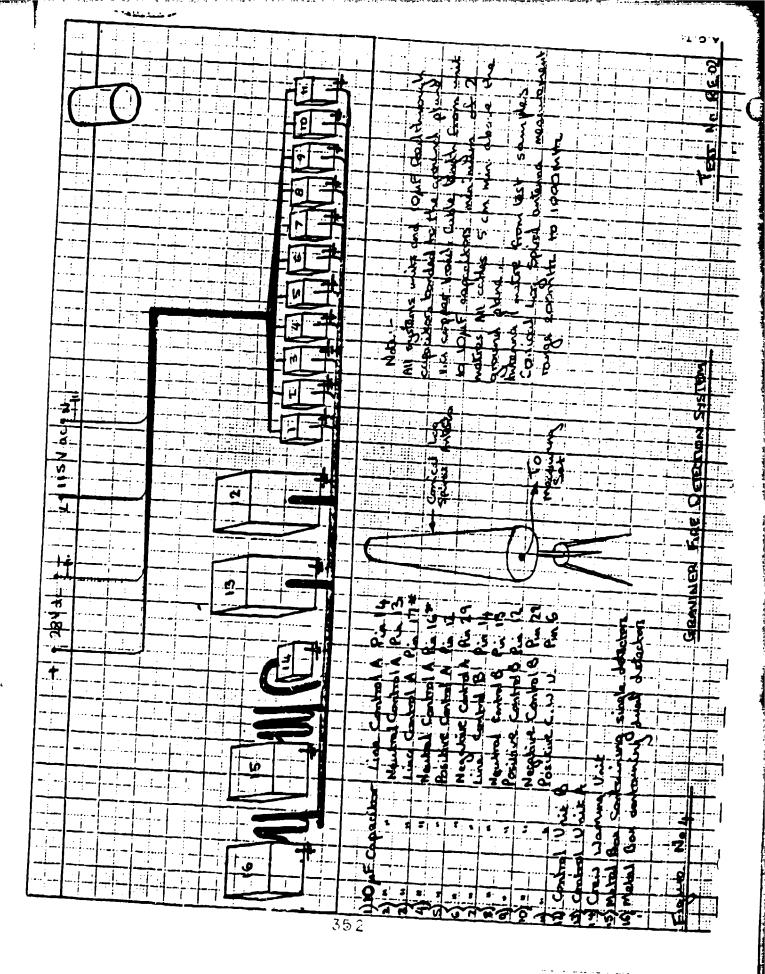
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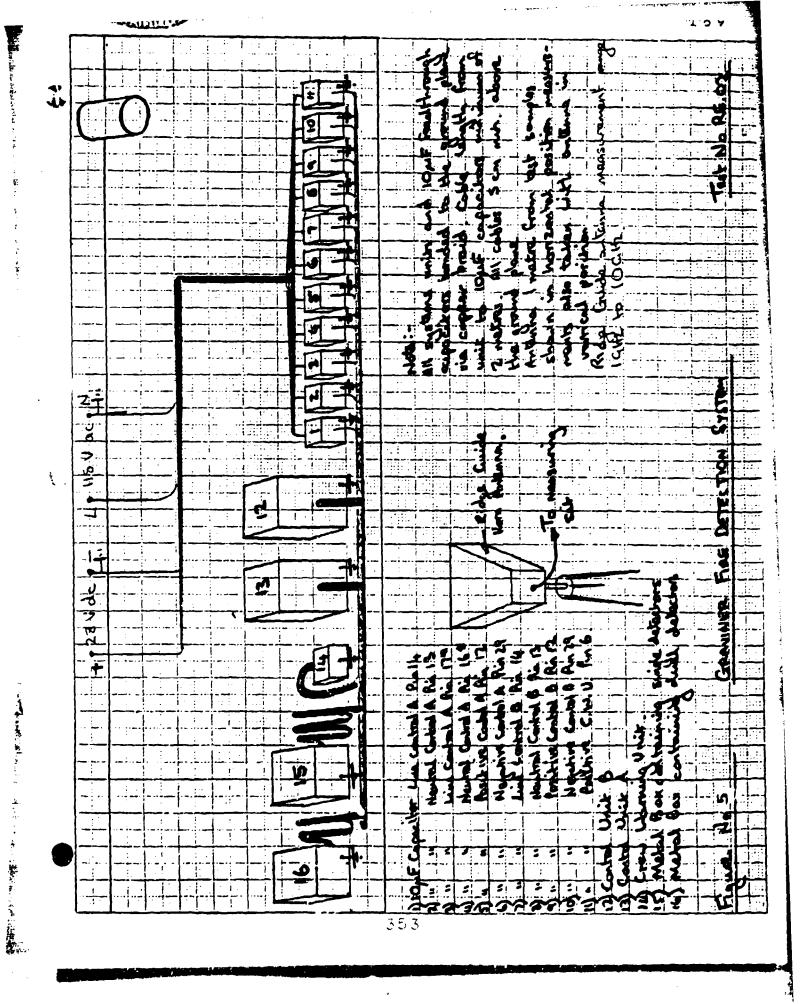
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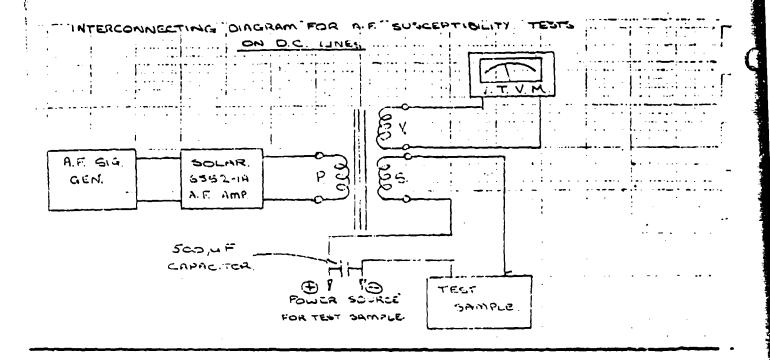


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INTERCONNECTING DIAGRAM FOR ALL SULLETTIGILITY TESTS

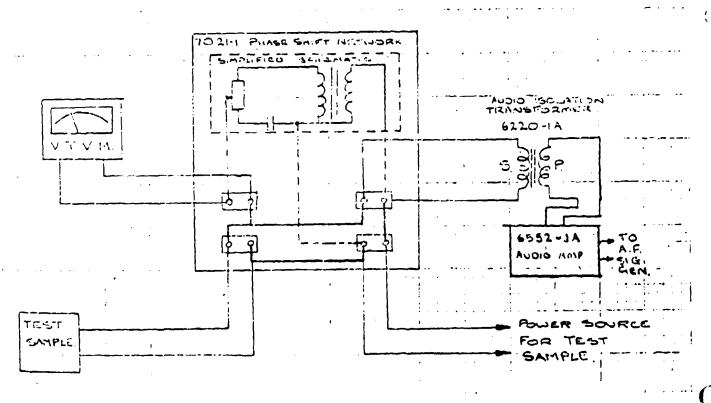


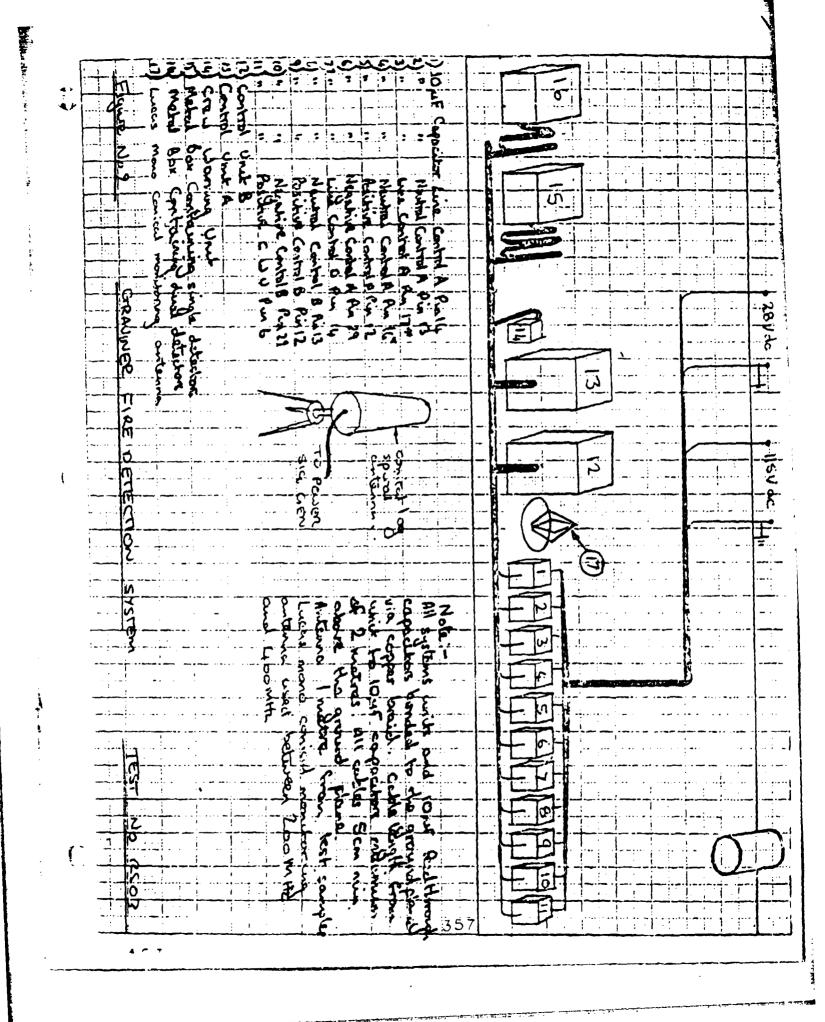
FIGURE No 6.

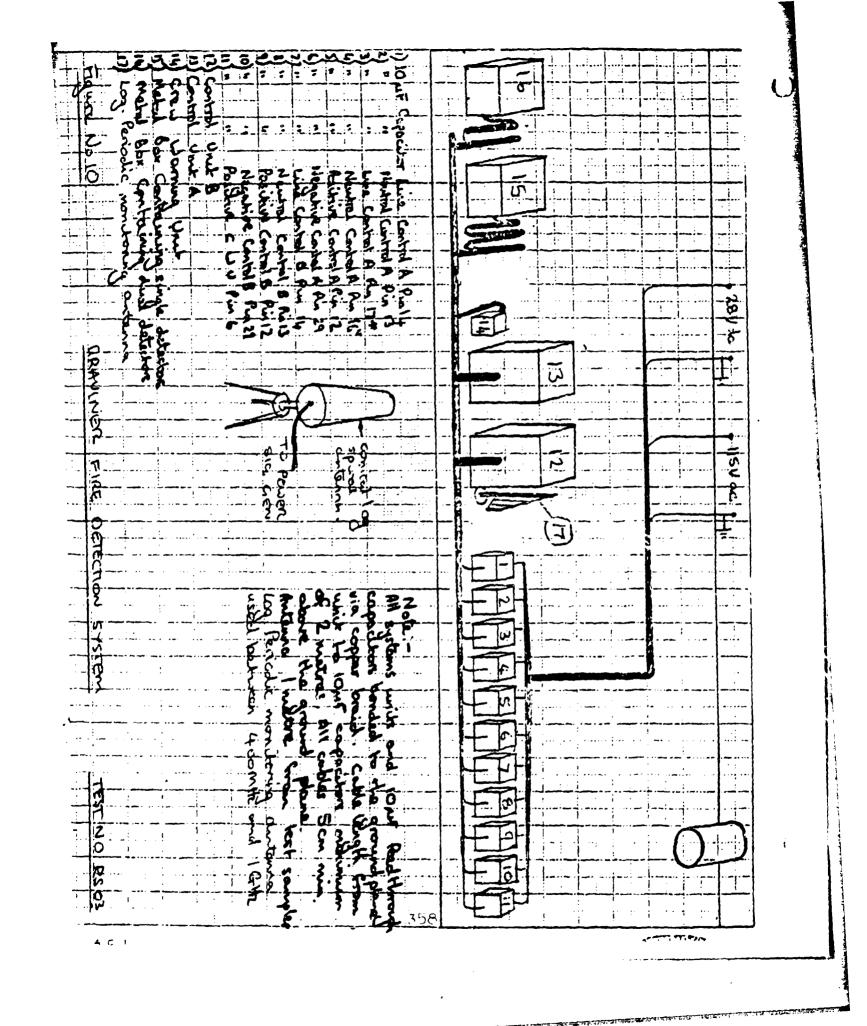
GRAVINER FIRE DETECTION

SYSTEM

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TEST No CS. OI





Appendix 2

Test Results

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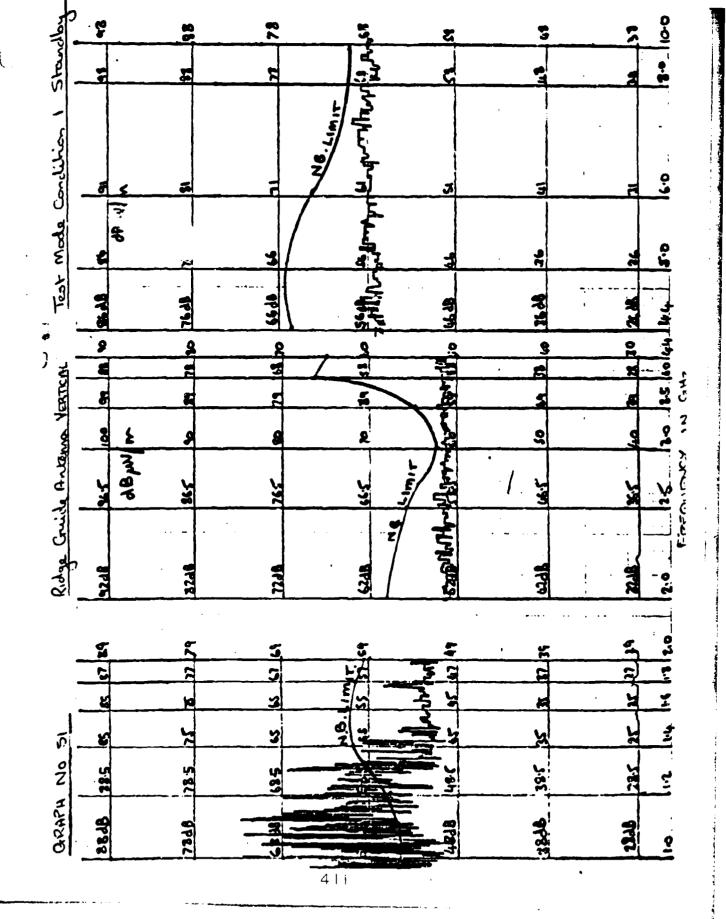
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Appendix 3

Test Sample Circuit Modifications

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Appendix 4

Test Equipment Data



MEASUREMENT STANDARDS LABORATORY

MARCONI INSTRUMENTS LIMITED Longacres St. Albans Herts. England

B.C.S approval no. 0006

Certificate of Calibration

Date of issue 6th February, 1980.

Serial no 04195

Page 1 ofpages

This certificate is issued in accordance with the conditions of the approval granted by the British Calibration Service. It is a correct record of the measurements made. Copyright of this certificate is owned jointly by the Crown and by the issuing laboratory. The certificate may not be reproduced other than in full, except with the prior written approval of the Director, B.C.S., and of the issuing laboratory.

A.D. Skinner. Head of Laboratory.

Tested for :

Lucas Aerospace Ltd.,

Maylands Avenue, Hemel Hempstead,

Herts.

Reference No. :

554315, 554317, 554318.

Order No. :

O/J/3144

Apparatus tested:

interference Analyser.

Model EMC-10. Serial No. 10471-E.

with Current Probe PCA-10.

Serial No. 471.

Fairchild Electro-Metrics Corp.

The ambient temperature was 20 $^{\circ}$ C ± 1 $^{\circ}$ C and the relative humidity was 50% $\pm 10\%$ RH.

Unless otherwise stated, the basis for estimating the limits of uncertainty quoted for the measurements shown, is the arithmetic summation of the relevant contributions.

The instrument was switched on for several hours before the tests were made to ensure that a stable operating temperature was reached. The tests were carried out in accordance with the procedures described in the instrument handbook supplied, the relevant paragraphs being quoted in each case.

123	continued
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Frequency calibration

The frequency calibration was tested as in para. 3.15.3(a) and the results are shown in Table 1.

Table 1

Digital	frequency	Measured frequency
indi	cator	
50.	H z	48.3 Hz
100	Hz	95.3 Hz
500	Hz	494 Hz
1	kHz	1.006 kHz
2 .	kHz	2.012 kHz
5	kHz	4.998 k Hz
10	kHz	10.000 kHz
20	kH:	19.974 kHz
50	kHz	49.864 kHz

The estimated limits of uncertainty of the measurement did not exceed ±1 Hz.

Amplitude calibration test

The amplitude calibration test was carried out as in para. 3.15.3(b) and the meter indication did not change by more than ± 0.5 dB.

Before the next test the control settings were changed to the following :

GAIN	Amplitude calibration
WB range	1 V
Selective range	1 V
Bandwidth	50 Hz

A 20 kHz test signal was applied to the receiver and the signal level was adjusted until the meter indicated 1 V. The voltage at the input was then measured and was 1.00 volts $\pm 0.1\%$.

Attenuator tests

The attenuator was tested as in para. 3.15.3(c) except that the impedance control was set to 50Ω . The results are shown in Table 2.

continued....

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SHEET. 2.

Table 2

Instrument	Nominal	Attenua	Estimated limits		
reading	attenuation dB	Wide band dB	50 Hz bandwidth dB	of uncertainty ±dB	
10 V	ref.	ref.	rel.	-	
1 V	20.0	20.0	20.0	0.1	
100 mV	40.0	40.0	40. 0	0.1	
10 mV	60.0	60.0	60.0	0.2	
l mV	80.0	80.0	80.0	0.2	
100 μV	100.0	100.0	•	0.5	

Meter scale shape

The meter scale shape was tested using the procedure shown in para. 3.15.3(j). The results are shown in Table 3.

Table 3

Meter scale shape

Scale mark	Measured attenuation
dB	dВ
0	ref.
3	3.0
6	6.0
10	9.8
15	15.2
20	19.6
25	24.6
30	29.8
35	35.6
40	39.9

The estimated limits of uncertainty for the scale shape measurements do not exceed ±0.1 dB.

Bandwidth tests

The 3 dB bandwidth of the analyser was measured on each bandwidth setting where the 3 dB changes were established against the laboratory standard attenuator. The analyser was tuned to 20 kHz. The results are shown in Table 4.

Table 4

Nominal bandwidth	Measured bandwidth
5 Hz	4.5 Hz ±0.1 Hz
50 Hz	53.6 Hz ±0.1 Hz
250 Hz	235.0 Hz ±0.1 Hz
	425

continued.....

Certificate of Calibration no. 04195. Page 4 of 4 pages

The tests listed below were made in accordance with the procedure in the manufacturer's handbook and were within the required specification limits.

Tangential sensitivity	para.	3.15.3(h)
Detector functions	para.	3.15.3(j)
Slideback operation	para.	3.8.6
Auto scan	para.	3.15.3(m)

Current probe

The current probe was connected to the instrument using a 62.5 cm length of coaxial cable. A test current was passed through a wire around which the current probe was clamped. The test current was adjusted to give a meter reading of 1 mV (equivalent to 1 mA). The result is shown in Table 5.

Control settings

As required for amplitude calibration
l mV
10 ki2
500 kHz
50 Hz
0
as necessary
CARRIER

Table 5 ·

Test frequency	Indicated current	Measured current
l kHz	1 mA	1.00 mA ±0.01 mA

The frequency response of the current probe was determined over the range 50 Hz to 50 kHz and the results are shown in Table 6.

Table 6

Freque	ency Response relative to 1	kHz The estimated limits of uncertainty do not exceed ±d
50 I	-1.5 dB	0.2
100 1	Hz -0.8 dB	0.1
200 I	Hz -0.1 dB	0.1
1 1	kHz 0 dB	0.1
* 21	kHz -0.1 dB	0.1
* 51	kHz -0.25 dB	0.1
* 101	kHz -0.75 dB	0.2
¥ 20 I	kHz -1.1 dB	0.2
* 501	kHz ~1,8 dB	0.2

^{*}These measurements are not within the scope of the Laboratory's prevailing approval but are reported herein for completeness.

Measurements made by .



exceed ±dB

FAIRCHILD EMC 25 MEASURING SET

TABLE 1.1. SENSITIVITY AND BANDWIDTH

•-	·	BANDWIDTHS (3db) (Nominal)					TY	
BAND	FREQUENCY RANGE	.1 NB	NB	W8	.1NB	NB	IMPULSE WB db/uV/MHz	
1	10.0 kHz - 35.0 kHz	50 Hz	500 Hz	4 kHz	.016	.04	+34	
2	35.0 kHz75.0 kHz	50 Hz	500 Hz	4 kHz	.016	.04	+33	
3	70.0 kHz — 150 kHz	50 Hz	500 Hz	4 kHz	.016	.05	+33	
4	120 kHz - 240 kHz	50 Hz	500 Hz	4 kHz	.016	.05	+33	
5	240 kHz 500 kHz	50 Hz	500 Hz	4 kHz	.016	.06	+33	
·6	0.5 MHz - 1.1 MHz	50 Hz	500 Hz	5 kHz	.016	.06	+32	
7	1.1 MHz - 2.4 MHz	50 Hz	500 Hz	5 kHz	.016	.06	+32	
8	2.4 MHz - 5.5 MHz	500 H₂	5 kHz	50 kHz	.03	.10	+22	
. 9	5.5 MHz - 12.5 MHz	500 Hz	5 kHz	50 kHz	.03	.10	+22	
10	12.5 MHz 30 MHz	500 Hz	5 kHz	50 kHz	.03	.10	+24	
11	20 MHz - 45 MHz	5 kHz	50 kHz	500 kHz	.22	0.6	+20	
12	45 MHz - 100 MHz	5 kHz	50 kHz	500 kHz	.22	0.8	+20	
. 13	100 MHz 200 MHz	5 kHz	50 kHz	500 kHz	.22	8.0	+20	
14	200 MHz - 500 MHz	5 kHz	50 kHz	500 kHz	.35	1.0	+23	
15	500 MHz - 1000 MHz	5 kHz	50 kHz	500 kHz	.50	1.6	+30	

NOTE: Tangential Sensitivity — defined as the internal noise level or as the input signal level required to raise the meter reading 3 dB above the instrument noise. Tangential Sensitivity level is at least 8 dB above minimum discernible signal (MDS), MDS is sometimes defined as being 0.5 dB above the noise level.

SHEET 5



MEASUREMENT STANDARDS LABORATORY

MARCONI INSTRUMENTS LIMITED Longacres St. Albans Herts. England

B.C.S approval no. 0006

Certificate of Calibration

Date of Issue 13th February, 1980.

Page 1 of?.....pages

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> A.D. Skinner. Head of Laboratory.

Tested for :

(.

Electro Metrica Ltd.,

84 Tile House Street,

Hitchin, Herts.

Order No. :

O/J/3144.

Reference No. :

554313.

Apparatus tested :

Interference Analyser.

Model EMC - 25 mk 3 Serial No. 366

Fairchild Electrometric Corp.

The ambient temperature was 20 °C ±1 °C and the relative humidity was 50% ±10% RH.

The basis for estimating the limits of uncertainty quoted for the measurements shown, is the arithmetic summation of the relevant contributions.

The instrument was tested at the 50 ohm coaxial input using a source of signals of 50 ohms impedance and having a waveform which approximated closely to a sine curve.

The instrument was tested at each of the frequencies shown in Table 1 in accordance with the following paragraphs. The function switch was set to 'CARR'.

Test 1.

With the tuning dial and range switch set to each frequency in turn, the input signal frequency was adjusted to produce a maximum reading on the meter and the measured frequency recorded in Table 1, Col. 2.

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Test 2.

The 6 dB bandwidth was measured by noting the total frequency change above and below the frequency recorded in Test 1, which resulted in a fall in a meter indication of 6 dB as established against the laboratory standard attenuator. The 6 dB bandwidth was measured on both the narrow and broad bandwidth settings. The results are recorded in Table 1, Cols. 4 and 5.

Test 3.

The 'calibration setting' was determined by applying an input voltage of $100 \,\mu\text{V}$ for ranges 1 to 10 and 1 mV for ranges 11 to 15 with the input attenuator set to 40 dB (BLACK) for ranges 1 to 10 and to 60 dB (RED) for ranges 11 to 15. The instrument gain control was then adjusted to give an indication on the meter of 0 dB. With the detector function switch set to 'PEAK' and the bandwidth control switched to 'wide' the 'shunt cal' button was pressed and the resulting reading on the meter noted and recorded as the calibration setting (dB μ V) in Table 1, Col. 3.

Test 4.

(==

The broadband correction factor in $dB_{\mu}V/MHz$ was determined on each range using an impulse generator type CIG 25 SN 120. The results of this test are shown in Table 1, Col. 7. The impulse generator was calibrated at the 70 $dB_{\mu}V/MHz$ and 90 $dB_{\mu}V/MHz$ settings before use. The calibration showed that the output was within ± 0.5 $dB_{\mu}V/MHz$ of the setting over the required frequency range. The repetition rate was set to 100 Hz.

Test 5.

For this test the receiver was first calibrated for direct reading signal levels in $dB_{\mu}V$ (see para. 3.3.1 CW CALIBRATION in the instrument handbook).

With the attenuator control set to the fully counter-clockwise position the input signal giving unity signal/noise ratio was measured by noting the input voltage which caused the meter noise reading to increase by 3 dB. The results of this test are shown in Table II.

Test 6.

The 6 x 20 dB steps of the input attenuator were compared with the laboratory standard attenuator at 30 MHz. The results are shown in Table III. For convenience the Black scale was used for these tests.

Test 7.

The scale shape of the meter was tested at 30 MHz and the result is shown in Table IV.

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continued

MEASUREMENT STANDARDS LABORATORY
Marconi Instruments Limited St. Albans
B.C.S. approval no. 0008

Certificate of Calibration no. 04171.

Page 3 of 7 pages

Table 1

	Frequency	Measured	Calibration	6 dB Ban	dwidth	Broad band
		frequency	setting	Narrow	Wide	correction factor
Band	kHz	kHz	dВ	Hz	kHz	dB _µ V/MH ₂
1	10	10.0	+1.0			
	14	14.5	+1.0			
	18	18.3	+1.0			
	22	22.3	0	880	5.80	. 43
	26	25.9	-0.5			
	30	30.0	-1.0			
	34	34.0	-1.0		•	
2	35	35.0	-1.0			
	40	40.8	-1.0			
	45	45.7	-1.0			
	50	50.3	-1.0			
	55	55.1	-1.0	890	5.62	43
	60	59.7	-1.0			
	65	64.9	-1.5			
	70 •	70.0	-1.5			
	75	75.2	-2.0			
3	70	68.2	-2.5			
•	80	79.9	-2.0			
	90	90.5	-2.0			
	100	99.2	-1.0			
	110	109.7	-1.0	870	7.31	43
	120	118.3	-1.0			
	130	128.3	0			
	140	139.1	+0.5			
	150	149.9	+0.5			
4	120	119.2	+0.5			
	140	141.8	+0.5			
	160	161.1	+0.5			
	180	181.6	+0.5	600	7.51	43
	200	199.1	+0.5			••
	220	219.5	0			
	240	238.8	0			
_	260	258.6	0			
5	250	249.4	-2.0			
	300	305.4	-2.0			
	350	354.2	-2.0	850	5.76	43
	400	400.7	-2.0	000	34 10	77
	450	450.1	-2.0			
	500	498.8	-2.1			

4 30

continued.....

Certificate of Calibration no. 04171.

Page 4 of 7 pages

Table I continued

		1	apre I continu	ica		
	Frequency	Measured frequency	Calibration setting	6 dB Ba Narrow	ndwidth Wide	Broad band currection
	MHz	MHz	dB	Hz	kHz	iactor
Band		••				dBµV/MHz
6	0.5	0.49	-2.5			
Ū	0.6	0.61	-2.0			
	0.7	0.71	-2.0			
	0.8	0.81	-2.0	790	6.31	43
	0.9	0.90	-2-0			
	1.0	1.00	-2.0			
	1.1	1.10	-2.0			
-						
7	1.2 1.4	1.19 1.42	-2.0 -2.0			
	1.6	1.61	-1.75			
	1.8	1.79	-1.75	900	6.10	44
	2.0	1.79	-2.0	700	0.10	44
	2.2	2.19	-2.0			
	2.4	2.40	-2.0	kHz		
	2.7	2.40	-2.0	KIIZ		
8	2.5	2.49	-2.0			
	3.0	3.01	-2.0			
	3.5	3.49	-2.0			
	4.0	3.99	-1.5	10.09	65.6	23
	4.5	4.43	-2.0			
	5.0	4.96	-1.75			
	5.5	4.94	-1.75			
9	6.0	6.01	-1.0			
-	7.0	7.04	-1.0			
	8.0	7.99	-0.5			
	9.0	9.01	0	9.98	66.0	24
	10.0	9.98	0			
	11.0	10.96	-1.0			
	12.0	12.00	-1.0			
10	14	13.99	-1.0			
10	14 16		_			
	18	16.02 17.85	0 0			
	20	19.77	0			
	22	21.49	Ö	10.02	69.4	25
	24	23.66	o	10.02	0). 1	23
	26	25.72	Ö			
	28	27.77	-0.5			
	30	29.86	0			
_						
11	20	19.72	-2.0			
	25	25.40	-1.0			
	30	30.18	-1.0	121.1	707.7	- 1
	35	35.01	0 . 4 3	. 1		
	40	39.75	-1.043	•		
	45	45.04	-1.0			

Certificate of Calibration no. 04171.

Page 5 of 7 pages

Table I continued

	Frequency	Measured frequency	Calibration setting	6 dB Ban Narrow	dwidth Wide	Broad band correction factor
Band	MHz	MHz	dВ	kHz	kHz	dB _µ V/MHz
12	50	50.41	0			
	60	60.59	+1.0			
	70	70.34	+1.5	101	7.5	
	80	79.93	+2.0	106.6	740. 2	+1
	90	89.57	+1.0			•
	100	100.00	+1.0			
13	100	99.8	+2.0			
	120	120.9	+2.5		•	
	140	141.3	+2.0		(55.5	
	160	160.7	+2.0	109.0	673.2	+2
	180	179.4	0			
	200	199.4	-1.0			
14	200	200.5	-1.0			
	250	255.7	-1.0			
	300	303.5	-2.0			
	350	352.1	-3.0	114.6	624.6	+2
•	400	399.3	-2.0			_
	450	448.1	-2.0			
	500	500.3	-2.0			
15	500	504.4	0			
	600	612.4	+1.0			
	700	708.1	+3.0			_
	800	805.5	+1.5	132.1	753.7	+1
	900	899.1	+1.0			
	1000	997.7	+1.0			

continued.....

Table II

Ranges	Input voltages for unity signal/noise ratio
1 - 5	Less than -27 dBuV
6 & 7	Less than -27 dBµV
8 & 9	Less than -20 dBµV
10	Less than -11 dBµV
11	Less than -5 dBµV
12	Less than -4 dBµV
13	Less than +1 dBµV
14	Less than 0 dBµV
15	Less than $+6 dB\mu V$

Table III

Switch setting (Black scale) (dB)	Attenuation relative to 40 dB position Frequency 30 MHz (dB)
0	-38.2
20	-20.0
40	ref.
60	+20.0
80	+40.0
100	+60.2

Table IV

Attenuator (dB)	setting	Meter reading (dB)
• •		
+20		+20.2
+18		+18.2
+16		+17
+14		+15
+12		+12.2
+10		+9.8
+8		+7.5
+6	•	+5
+4		+3.5
+2		+2
0		ref.
-2		-2.4
-4		- 5
-6		-7. 2
-8		-9
-10		-10
-12		-11
-14		-13
-16		-16
-18		-18
-20	43	
-30		-30.5
-40		-39.5

MEASUREMENT STANDARDS LABORATORY
Marconi Instruments Limited St. Albans
8.C.S. approval no. 0006

Certificate of Calibration no. 04171.

Page 7 of 7 pages

€.

The estimated limits of uncertainty of the measurements did not exceed the following:

for frequency:

±1.0%.

for bandwidth:

(

narrow wide

ranges 1 to 7 ±30 Hz ±100 Hz ranges 8 to 10 ±100 Hz ±1 kHz ranges 11 to 15 ±1 kHz ±10 kHz

for calibration settings : ±0.5 dB.

for attenuation and meter scale law: ±0.5 dB.

The insertion loss of the three coaxial cables fitted with type TNC male connectors was measured at the frequencies shown in Table V.

Table V

Cable No./length	Frequency MHz	Insertion loss dB	Estimated limits of uncertainty ±dB
CAC-25 RG223	1	0.08	0.02
7.52 metres	30	0.54	0.02
	500	2.73	0.1
	1000	3.85	0.1
CAC-25 RG223	1	0.09	0.02
	30	0.56	0.02
	500	2.70	0.1
	1000	3.89	0.1
CAC-25 RG223	1	0.10	0.02
7.95 metres	30	0.57	0.02
	500	2.87	0.1
	1000	4.17	0.1
CAC-15 RG223	1	0.09	0.02
	30	0.58	0.02
	500	2.94	0.1
	1000	4.29	0.1

Measurements made by: R. Javell

---- END ----



MEL Industrial Limited

CALIBRATION REPORT No. 2018

INSTRUMENT 60d8 Step	Attenuator	CUSTOMER & ADDRESS
TYPE No. 90389-3	SER. No.	Lucas Aerospuce,
MANUFACTURER	Singer	Hemel Hempstead.
CAL DATE	4.3.80	
RECOMMENDED RECALIBRATION DATE	4.9.80	

CALIBRATION

			···		
Attenuator .		Actual Att	enuation (dB)		
Setting (dB)	10Hz	1MHz	100MHz .	1 GHz	
3	2.9	2.9	2.9	3.0	
6	5.8	5.9	5.9	6.3	
10	11.1	11.1	11.6	11.2	
20	20.0	20.0	20.3	20.0	
30	30.2	30.2	30.1	30.2	
60	60.8	61.0	61.2	60.8	

Cal Lab has 052	4 (0526) app	roval cert r	0.71990/ 1/0	01	
All measurement	s are tracea	ble to natio	onal standard v	via B.C.S.	
			435		
				Sheet 13	
					



REL Industrial Limited

CALIBRATION REPORT No. 2020

Radio Interference INSTRUMENT Analyser Receiver		CUSTOMER & ADDRESS
TYPE No. NM 65T	SER. No. 145	Lucas Aerospace,
MANUFACTURER	Singer	Hemol Humpstead.
CAL. DATE	5.3.80	
RECOMMENDED RECALIBRATION DATE	5.9.80	

CALIBRATION

Meter Sca	le Shape (Tracking Accu	racy)	
qr	Field Intensity	Direct Peak	Slidoback Peak
0	0.5	2.5	2.5
10	10.0	10.1	10.1
20	20.0	20.0	20.0
30	30.5	30.1	30.1
40 ref	40.0	39.9	39.9
50	50.0	49.5	
60	59.0	58.8	55.8
Attenuato	r Accuracy	Output Sockets	
dB	Meter Reads	X O/P Single Ban	nd 1.0V to 10.36V
0 ref	40.0	X O/P Multiple B	3and 1 0.97V to 3.29V
+ 20	39.2		3and 2 3.88V to 6.5V
±_40	39.2		Band 3 6.81V to 9.92V
+ 60		Y_0/P_7.395V	
		Video Linear O.	4V pk-pk
		Stretched Linear	1.65V pk
		Pulse Width 0.5	m 'sec
		Audio 🗸	
		436	
			SHEET 14
CALIBRATED	AY		APPHOVEC HY

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Dial	Actual	Cal.	Sensi	tivity	keserve
req.	Freq.	Figures	NB	нв	Gain
(z	GHZ	(18	dB refer	red 10 luV	dR
and 1					
.0	1.002	41.5	0	25.5	17.0
5	1.502	41.0	0	22.0	20.0
. 0	2.003	41.4	0	24.0	20.0
ind 3					
زن.	2.059	43.0	3.0	32.5	15.0
. 5	2.508	43.0	0	28.0	15.5
. 0	3.007	42.5		28.5	15.0
.5	3.510	42.0	Ů	28.0	16.2
.0	4.001	41.5	3.5	33.0	11.0
.1	4.493	40.5	5.5	35.0	9.5
and 3					
. 4	4.406	40.5	9.0	38.0	. 13.0
.0	5.008	39.8	9.1	38.5	13.2
<u>.s</u>	5.507	40.0	12.0	41.0	U.O
.0	6.014	38.6	14.5	14.0	10.0
. 5	6.516	38.2	8.0	37.6	15.8
.0	7.022	18.0	9.5	38.5	15.0
. 5	7.516	38.0	11.2	41.0	13.5
.0	4.020	38.0	7.5	37.0	16.0
.5	8.518	37.5	6.5	36.0	17.0
. ()	9.016	35.0	6.4	35.5	18.0
کہ	9-520	34.5	5.0_	34.0	19.5
	10.011	34.2	6.0	35.0	13.0

RELL INDICTRIAL ITA

CALIBRATION REPORT No.

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700		SHEET 16.	
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REL Industrial Limited

CALIBRATION REPORT No.

2019

INSTRUMENT 6' Transmission Lead		CUSTOMER & ADDRESS	
TYPE No. 92194	SER. No	Lucas Aerospace,	
MANUFACTURER	Singer	Hemel Hempstoad.	
CAL. DATE	5.3.80		
RECOMMENDED RECALIBRATION DATE	5.9.80		

CALIBRATION

	Frequency	Logs dB
	GH2	
	1	- 0.6
	2	1.0
	3	- 1.4
	4	- 1.6
	6	- 1.A. - 2.2
	7	- 2.2
	8	~ 2.6
	9	- 2.9
•	10	- 3.6
		
	Cal Lab has 0524 (0	526) approval cert no. 71990/1/01
	All measurements ar	e traceable to national standard vis B.C.S.
	and a second the second to respect to section which we see a section of the contract of the second to the second t	
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	and the first considerable of the second	439
		SHEET 17

1996



REL Industrial Limited

CALIBRATION REPORT No.

INSTRUMENT Current Probe		robe	CUSTOMER & ADDRESS
TYPE No.	91197-1	SER No. BG 72	Lucas Aerospace,
MANUFACTU	IRER		Hemel Hempstead.
CAL. DATE		12.2.80	
RECOMMEND RECALIBRAT		12-4-80	

CALIBRATION

	CALIE	SKATION	
Frequency	27	dB Above or	
	Ohas	Below 1 ohm	
30 11/2	0.006	- 44.44	
100 Hz	0.03	- 30.46	
200 Hz	0.06	- 24.44	
500 Hz	0.14	- 17.08	
1 KHz	0.24	- 12.40	
2 KHz	0.32	- 4.90	
5 KHZ	0.38		
10 KHz	0.38	- 8.40	
20 KHz	0.38	8.40	
50 KHz	0.36	- 8.87	
100 KHz	0.37	- 8.64	
200 KHz	0.38	- 8.40	
500 KHz	0.38	- 8.40	
1 MHz	0.36	- 8.87	
2 MHz	0.35	- 9.12	
5 MHz	0.30	- 10.46	
8 MHz	0.19	- 14.42	
		440	
		SHEET 18.	



REL Industrial Limited

CALIBRATION REPORT No. 1997

INSTRUMENT Current P	robe.	CUSTOMER & AUDRESS
TYPE No. 91550-1	SER. No. 912-130	Lucas Aerospace,
MANUFACTURER	Stoddart	Hemel Hempstend.
CAL DATE	12.2.80	·
RECOMMENDED HECALIBRATION DATE	12.3.30	

	- OALIE	
C	77	dB Above or
Frequency	ZT	
MHz	Ohms	Below 1 Ohm
0.01	0.16	- 15.92
0.02	0.29	- 10.75
0.05	0.72	- 2.85
0.1	1.2	1.58
0.2	2.3	7.23
0.5	4.5	13.06
1.0	5.2	14.32
2.0	5.6	14.95
5.0	6.0	15.56
10.0	5.5	14.81
20.0	5.5	14.81
50.0	4.4	12.87
60.0	4.4	12.87
70.0	4.2	12.46
80.0	3.0	9.54
90.0	3.4	10.63
100.0	3.4	10.63
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REL Industrial Limited

CALIBRATION REPORT No.

1973

INSTRUMENT EFS/LMT/LDI		CUSTOMER & ADDRESS
TYPE No.	SER. No. 056/011	Lucas Aerospace,
MANUFACTURER	IFI	Remel Hempstead.
CAL. DATE	20.12.79	
RECOMMENDED RECALIBRATION DATE	20.6.80	

	Input	EFS Hater Reading	LDI Meter Reading
	Volts/Range-	Volts/Hetre	Volts/Metre
	3 Volt Range	3 Volt Range	3 Volt Range
_	1.0	1.0	1.0
	· 1.5	1.5	1.5
	2.0	2.0	2.0
_	2.5	2.49	2.49
_	3.0	3.0	3.0
	10 Volt Range	10 Volt Range	10 Volt Range
	3.0	3.0	3.0
	4.0	4.1	4.0
_	5.0	5.2	5.0
	6.0	6.2	6.0
_	7.0	7.1	7.0
	8.0	8.0	8.0
	9.0	9.0	9.0
	10.0	10.0	10.0
	Cal Lab has 0524 (05	326) approval cert no. 71990/1,	/01
_	All measurements are	traceable to national standar	d via B.C.S.
		442	SUPET ON



MEL Industrial Limited

CALIBRATION REPORT No. 1974

INSTRUMENT EFS/LMT		CUSTOMER & ADDRESS
TYPE No.	SER. No. 055	Lucas Aerospace,
MANUFACTURER	IFI	Remel Hempstead.
CAL. DATE	20.12.79	·
RECOMMENDED RECALIBRATION DATE	20,6,80	

	CALIB	HATION	
3	Input	EFS Meter Reading	
	Volts/Range	Volta/Netre	
	3 Volt Range	3 Volt Range	
	1.0	1.05	
	1.5	1.5	
	2.0	2.0	
·	2.5	2.5	
	3.0	3.0	
	10 Volt Range	10 Volt Range	
	3.0	3.0	
	4.0	4.0	
	5.0	5.1	
	6.0	6.1	
	7.0	7.1	
	8.0	8.1	
	9.0	9.0	
	10,0	10.0	;
Cal La	b has 0524 (0526) approval c	ert no. 71990/1/01	
All me	asurements are traceable to	national standard via B.C.S.	
		443 SHEET 21	
	5 P Mead		



REL Industrial Limited

CALIBRATION REPORT No. 1976

INSTRUMENT Levelling	g Рге-А п р	CUSTOMER & ADDRESS
TYPE No. LPA-I	SER. Nº 0374942	Lucas Aerospace,
MANUFACTURER	I.F.I.	Hemel Hempstead.
CAL. DATE	4.1.80	
RECOMMENDED RECALIBRATION DATE	4.7.80	

_	E.F.S. Meter .	LPA-I Heter	Reading
	Reading	Channel A Unit A	Channel B Unit I
	Volts/Metre	Volts/Netre	Volts/Hetre
	3 Volt Range		
	1.0	1.0	0,9
_	1.5	1.5	1.45
_	2.0	1.99	1.9
_	2.5	2.5	2.44
	3.0	3.0	3.0
	10 Volt Range		
	3.0	3.0	3.0
	4.0	4.0	4.0
	5.0	5.0	4.9
	6.0	5.9	5.9
	7.0	7.0	6.9
	8.0	8.0	7.8
	9.0	9.0	8.8
	10.0	10.0	10.0

MARCONI INSTRUMENTS LIMITED

SERVICE DIVISION

Electrical and Electronic Calibration Laboratories The Airport, Luton, Beds. LU2 9NS Telex: 825248

Telephone: Luton 33866

Def Stan. 05-24/2

Registration No. 13 LM 01

Certificate of Test

This certificate is issued in accordance with our Order Acknowledgment, and the general terms and conditions of business of Marconi Instruments Limited. The M I. 90 day Warranty, details of which are given overleaf, applies only to the repairs carried out.

The equipment described below has been calibrated and found to comply with the manufacturer's published performance specification at the measured points, due allowance having been made for the uncertainty of the measurements.

Job No.

630490/3

Description

Signal Generator TF. 144H/-4

Serial No.

53698-12

c/w. 13 Amp Plug & Lead

The calibration was carried out using working standards which are subject to regular periodic verification, and the measurements are traceable to National Standards, except where none exist.

The calibration was carried out in accordance with the general requirements of Def. Stan. 05–26/2, using working standards which are subject to regular periodic verification, and the measurements are traceable to National Standards, except where none exist.

-

Periodicity 12 Konths

CALIBRATED TO: EHO35 1352

Date 19 2 80

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MARCONI INSTRUMENTS LIMITED SERVICE DIVISION

Electrical and Electronic Calibration Laboratories
The Airport, Luton, Beds, LU2 9NS
Telephone Luton 33866
Telex, 825248

Det Stan U5-24/2

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The equipment described below has been calibrated and found to comply with the manufacturer's published performance specification at the measured points, due allowance having been made for the uncertainty of the measurements.

Job No

614285

Description

Signal Concrator TF. 8010/1

Serial No

53599/24 c/w. Mains Lead a 13 Amp Plug

The calibration was carried out using working climbachs which are subject to regular periodic verification, and the measurements are traceable to National Standards, along towhere more exist.

The calibration was carried out in accordance with the general requirements of Def. Stan. 05–26/2, using working standards which are subject to regular periodic verification, and the measuraments are traceable to National Standards, except where none exist.

Remarks

CALIBRATED TO MAN. SPEC.

Signed Olan Sales

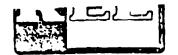
for Quality Manager, Service Division

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SHEET 24



REL Industrial Limited

CALIBRATION REPORT No. 1930

INSTRUMENT Power Si	gnal Source	CUSTOMER & ADDRESS
TYPE No. C203	SER. No. 125	Lucas Aerospace,
MANUFACTURER	A)·IL	Homel Hempstead.
CAL. DATE	26.9.79	
RECOMMENDED RECALIBRATION DATE	,	• .

Frequency	Dial	Neter 100W	·	Heter 50W	
		Monitor O/P	O/P Power	Monitor O/P	O/P Power
:00	3160	No Coupler		No Coupler	·
250	5580	+ 17 dBm	45W	+ 17 dBm	45W)
300	7220	+ 16 "	50W	+ 16 "	50W)
350	8230	+ 16 "	50W	+ 16 3 11	50W)
400	9100	+ 15 "	50W	+ 15 "	50W)
450	9790	+ 15"	50W	+ 15 **	50W)
7051AH				· .	
.		Heter 80V		Moter 40V	
450					
475	3520	+ 17 dBm	.40V	+ 14,4 dBm	20W
500	3790	+ 17 "	52W	+ 14.4 "	25¥
525	4050	+ 17.8 dBm	54V	+ 14.5 "	26V
550	4260	+ 18.0 "	54¥	+ 14.6 "	26Y
57-	4480	+ 18.5 "	58V	+ 15.2 "	27V
600	4660	+ 18.5!!	58Y	+ 15.2 "	27V
625	4840	+ 19.0 "	GOV	+ 15.6 "	28¥
650	5000	+ 19.2 "	60V		29V
675	5170	+ 19.2 "	62V	+ 16.0: "	بر ۲۵۳
700	5520	+ 19.5 "	, 63W	+ 16.2 "	30V
725	. 5430 5540	·+ 19.2 " .	60¥ 55 85	16.2	28V

	,			•		
7051BH			~ ~~~~~~			
Frequency	Dial	Heter 50W				
		Monitor O/P	O/P Power			
750	7650	+ 17.6 dBm	47W	•		
300	8130	+ 17.6 "	47W			
350	8540	+ 18.0 "	49W		•	•
900	8920	+ 18.3 "	49W			
950	9250	+ 18.5 "	49¥			
1000	9560	+ 18.6 "	48W			
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CALIBRATION REPORT No. 448

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MARCONI INSTRUMENTS LIMITED SERVICE DIVISION

Electrical and Electronic Calibration Laboratories
The Airport, Luton, Beds, LU2 9NS
Telephone, Luton 33866
Telex 825248

Def. Stan. 05-24/2

Registration No. 13 LM 01

Certificate of Test

This certificate is issued in accordance with our Order Acknowledgment, and the general terms and conditions of business of Marconi instruments Limited. The M.I. 90-day Warranty, details of which are given overleaf, applies only to the repairs carried out.

The equipment described below has been calibrated and found to comply with the manufacturer's published performance specification at the measured points, due allowance having been made for the uncertainty of the measurements.

Job No.

630490/8

Description

Voltmeter TF. 1041B

Serial No.

JA 217-484

c/w. 2 Probes & Leads & T Connector Unit

The calibration was carried out using working standards which are subject to regular periodic verification, and the measurements are traceable to National Standards, except where none exist."

The colibration was carried out in accordance with the general requirements of Def. Stan. 05–26/2, using working standards which are subject to regular periodic verification, and the measurements are traceable to National Standards, except whore none exist.

Hemarks

Periodicity 12 Months

EH. 006. 153. III

Signed Costart Service Division

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SHEET 28

I I HELL COM instruments

MARCONI INSTRUMENTS LIMITED SERVICE DIVISION

Electrical and Electronic Calibration Laboratories

The Airport, Luton, Beds. LU2 9NS

Telephone: Luton 33866

Telex: 825248

Def Stan 05-24/2

Registration No. 13 LM 01

Certificate of Test

This certificate is issued in accordance with our Order Acknowledgment, and the general terms and conditions of business of Marconi Instruments Limited. The M I. 90-day Warranty, details of which are given overleaf, applies only to the repairs carried out.

The equipment described below has been calibrated and found to comply with the manufacturer's published performance specification at the measured points, due allowance having been made for the uncertainty of the measurements.

Job No.

630490/9A

Description

Electronic Voltmeter TF. 2604

Serial No.

200933-037

c/w. 2 Probes & Leads TH 5031B

+ 13 Amp Plug & Lead

The calibration was carried out using working standards which are subject to regular periodic verification, and the measurements are traceable to National Standards, except where none exist.

The calibration was carried out in accordance with the general requirements of Def. Stan. 05-26/2, using working standards which are subject to regular periodic verification, and the measurements are traceable to National Standards, except where none exist.

Periodicity 12 Months

1. - F/-10451254

for Quality Manager, Service Division

451

SHEET 29

Appendix 5

TRANSIENT & SPIKE REPORT
AED/ENV/480550

Lucas Aerospace

Electrical Division

LABORATORY REPORT

GRAVINER LTD.

SLOUGH.

ADVANCED AIRCRAFT FIRE DETECTION SYSTEM :-

CONTROL UNIT TYPE 53813-203 SERIAL No 100
CONTROL UNIT TYPE 53813-204 SERIAL No 100
CIEN WARNING UNIT TYPE 53813-202

TESTS CSOE, RSO2 TO MIL-STD-461A.

TRANSIENT VOLTAGE ACCEPTANCE TO MIL-STD-704A.

Leeds Old Road West Yorkshire Bradford BD38LA

England



WORKING NUMBER

A570401E

CUSTOMER

Graviner Ltd, Elough.

CUSTOLER'S EQUIPMENT

Advanced Aircraft Fire Detection Syst :

Control Unit Type 53813-203 S/K 100. Control Unit Type 53813-204 S/K 100. Crew Warning Unit Type 53813-202.

CUSTOMER'S REQUIREMENTS

The system is to be subjected to test. CSO6, RSO2 to Speciation MIL-STD-461A Tests for transient voltage acceptanc to be applied to the requirements of MIL-STD-704A for category "B" Equipme :

CUSTOPER'S REFRESENTATIVE

Mr A. Mackrell.

TESTED BY

G. Mitchell.

DATE OF TESTS

April 1980.

TEST LOCATION

Environmental Laboratories, Bradford.

TEST EQUIPMENT

Pulse Generator Type AE 7753
Pulse Generator Type AE 7746
Oscilloscope Type 180A Serial No M2370, calibrated on each day of test.

1. INTRODUCTION

Tests were performed on the Advance Fire Detection System in accordance with the requirements of paragraphs 1.2.7.,1.2.9. and 1.2.11. of Messrs.

Graviner Ltd E.M.I. Test Plan (Issue No 4). The tests were performed in order to demonstrate the system compliance with Tests CSO6, RSO2 to MIL-STD-461A, Notice No 3, Class A1 and MIL-STD-704A.

2. TEST ARRANGEMENT

2.1. TEST LAYOUT

The test layout was as shown in figure No 1 of the test plan.

2.2. OFERATION OF THE SYSTEM

2.2.1. CONDITION 1 "STAIDBY"

This condition was when the U.V. source was switched off and the "FIRE" and "FIRE DET FAIL" indicators were not illuminated.

2.2.2. CONDITION 2 "FIRE"

This condition was when the U.V. source was switched on and the "FIRE" indicators were illuminated on the crew warning unit.

2.3. SUSCEPTIBILITY CRITERIA

The criteria for susceptibility/non-susceptibility was as follows :-

CONDITION 1 - Illumination of any Crew Warning Unit "FIRE" and "FIRE DETECT FAIL" indicators.

CONDITION 2 - Cancellation of either "FIRE" indicators.

2.4. TEST FROCEDURE

2.4.1. TESTS FOR TRANSIENT VOLTAGE ACCEPTANCE TO MIL-STD-704A.

2.4.2. POWER LEAD CONNECTIONS FOR TRANSIENT ACCESTANCE.

For the purposes of transient voltage acceptance the power cubies were linked as follows and treated as a single cubie.

457

(1)	115V	400Hz	Line to	Control Unit "A" Pin 14.)
	115V	400Hs	Line to	Control Unit "A" Pin 17.) all linked together
	115V	400Hz	Line to	Control Unit "B" Fin 14.)
(2)	115V	400Hz	Neutral	to Control Unit "A" Fin 13.)
	1157	400liz	Heutral	to Control Unit "A" Fin 17.) all were linked together
	1158	400Hz	Keutral	to Control Unit "B" Fin 13.)
(3)	28 V	D.C.	Positive t	co Control Unit "A" Pin 12)
	28V	D.C.	Positive t	o Control Unit "B" Pin 12) all linked together
	2,87	D.C.	Positive t	o Crew Warning Unit Pin 6)
(4)	28 v	D.C.	Negative 1	o Control Unit "A" Pin 29)
	28 V	D.C.	Negative t	o Control Unit "B" Pin 29) linked together

2.4.3. TESTS FOR TRANSIENT ACCEPTANCE TO A.C. POWER LEADS

The following step functions were selected from figure No 3 of MIL-STD-704A for category "B" equipment.

The step functions were applied with the system operating in the "STANDBY" mode and then repeated whilst in the "FIRE" mode. The results of the tests are shown below :-

STANDBY MODE			
BASIS OF STEP FUNCTION	APPLIED TIME VOLTAGE FERTOD RUMARKS		<u>rumarks</u>
Limit No 1 1 2 3 3 4 4 4	180V 149 160 60 Zero 102 Zero	0.1 SEC. 1.0 0.04 9.05 0.05 7.0 7.0	Not Susceptible
6	74 4 5 8	1	J.

	OF-WAR MODE		
BASIS OF STEF FUNCTION	AFFLIED VOLTAGE	TIME FERIOD	REMARKS
Limit No 1	180	0.1 SEC.	Not Susceptible
1	148	1,0	Not Susceptible
2	160	0.04	Not Susceptible
3	60	0.05	Both "FIRE" lights extinguish
3	Zero	0.05	and relight on resumption of the normal 115V surply
4	102	7.0	Not Susceptible
4	Zero	7.0	"PIRE" lights extinguish and fire detect fail become illuminated and extinguish after the transient and fire lights re-illuminated.
5	140	0.02	Not Susceptible
6	74	0.02	Cocasional R.H. fire lamp
			extinguishes but re-illuminates.

2.4.4. TESTS FOR TRANSIENT ACCEPTANCE TO D.C. POWER LEADS.

The following step functions were selected from figure No 9 of MIL-STD-704A for category "B" equipment.

CYCLE No	APPLIED VOLTAGE	Tike Feriod
1	80	0.06 SEC
2	49	1.0
3	70	0.02
4	60	0.015
5	11	0.03
6	8	0.05
7	2ero	7.0
8	12.5	7.0

The system was set to operate in the standby mode. Test cycle No 1 was then applied. This application caused both the "FIRE" lamps to fail.

The unit was examined by the customer's representative and it was found that k36, (150 1/2 % resistor), in both common logic boards had gone open circuit.

These components were then replaced with type W21 resistors, (150 2.50), resistors. The unit then operated satisfactorily.

The step functions were then applied with the system operating in the "STANDBY"mode and then repeated with the system operating in the "FIRE" mode.

The results of the tests are shown below :-

Cycle	<u>REMARKS</u>			
Cycle No	STANDBY MODE	OPERATE FOLE		
1 2 3 4	Not Susceptible			
5 6 7	not susceptible	Both "FIRE" lamps extinguish then relight following the transient. Both lamps dim for 7 seconds		

2.5. TESTS WITH IMPORTED VOLTAGE SPIKES ON D.C. POWER LINES

Paragraph 5.2.3. and figure 17 of KIL-STD-704A calls up an. imported voltage spike test for d.c. powered equipment. The spike is to be in the form of a single half sine wave of base width 10 μ S. The spike is to be superimposed onto the d.c. power leads. The amplitude of the test spikes is to be \pm 600 volts when at open circuit. The source impedance of the spike generator is to be 50 μ .

The +600v spikes were applied at a rate of one pulse per second to the d.c. lines. The system was then operated for a five minute period in each of the two operating modes. This procedure was then repeated with the polarity of the test spikes reversed.

Then on line then the amplitude of the positive going spikes was attenuated to +400 volts. The negatively imposed spikes were unattenuated.

The Fire Detection by stem operated normally throughout the application of these tests.

2.6. TEST CSO6 - CONDUCTED SUSCEPTIBILITY - POWER LEADS

2.6.1. TEST CSO6 - D.C. POVER LEADS

The spikes were parallel injected onto the d.c. power lines by means of the pulse generator type AE7746. The base width of the spikes was 10µS and the amplitude was set to twice the line voltage of 28 volts which = 56 volts. The total peak voltages in the case of positive and negative superimposed voltage spikes was +84 and -28 volts respectively with respect to the zero voltage level. The spike repetition frequency was set to ten pulses per second and the test was applied for a period of five minutes in each polarity for each operating mode.

The Fire Detection System operated normally throughout the application of the tests.

2.6.2. TEST CSO6 - A.C. POWER LEADS

The spikes were parallel injected onto the a.c. power lines by means of the pulse generator type AE7746. The base width of the spikes was $10\mu S$ and the amplitude of the spikes was set to 100 volts. The spike repetition frequency was set to ten pulses per second.

The spikes were synchronised to the power line frequency and positioned at each 90° position for a period of five minutes. The spike was also positioned from 0 to 360° of the power line waveform.

Positive and negative spikes were applied for equal time periods at all the phase positions listed above. The total time that the spikes were applied was not less than 30 minutes. This test was performed in the standby mode and then repeated for the fire mode.

The fire Detection System operated normally throughout the artification of the tests.

2.7. TEST RSO2 - SUSCENTIBILITY TO MECHATICALLY INLUCED FISIDS 2.7.1. CABLE TEST

Engretic Induction field tests were performed on all the cable bundles interconnecting the system. This bundle was wrapped with wire along the length of the bundle at a rate of two turns per metre length. The following tests were then applied:

- Test (a) A current of 20 Amps r.m.s. 400 ms passed through the wire.
- Test (b) Voltage spikes were applied to the wire at a rate of 10 pulses per second. The spikes were of a base width of 10µS and peak voltage 400 volts when measured across a 50 impedance in series with the wire wrappings.
- Test (a) was applied for a period of 5 minutes with the Fire Detection system operating in the standby mode. This procedure was then repeated with the system operating in the fire mode.

Test (b) was then applied to the wire whilst the system was operated for a period of 5 minutes in each of the two operating modes. These tests were then repeated with the polarity of the spikes reversed. The Fire Detection System operated normally throughout the application of the tests.

2.7.2. CASE TEST

2.7.2.1 CASE TEST - CREW WARNING UNIT

The case of the Crew Warning Unit was wrapped with three turns of wire as shown in figure (a) of Appendix "A" of this report. Tests (a) and (b) as detailed in paragraph 2.7.1. of this report were then applied to the wire wrapping.

2.7.2.2. CASE TEST - CONTROL UNIT TYPE 5351 3-203

The case of the control unit was wrapped with wire in a similar manner as described in para. 2.7.2.1. of this report. Tests (a) and (b) were then applied.

2.7.2.3. CASE TEST - CONTROL UNIT TYPE 53813-204

The case of the control unit was wrapjed with wire in a similar manner as described in para. 2.7.2.1. of this report. Tests (a) and (b) were then applied.

RESULTS

The Fire Detection System operated normally throughout the application of the tests.

3. CONCLUSIONS

The system was damaged by the application of the 80 volt transient acceptance requirement of MIL-STD-7C4A. This was due to the failure of R36.(1/2 W resistors).

Components R36 were replaced by type W22, (2.5 hatt resistors) and the acceptance tests were then satisfactorily completed. The system then operated normally throughout the tests and was not susceptible in any way to the test applications.

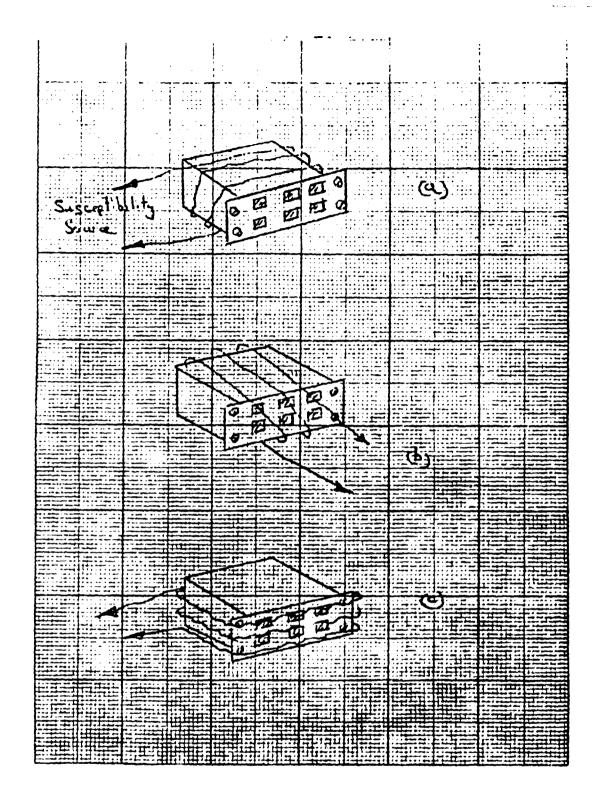
4. RECOMMENDATIONS

That the build standard of the units incorporates the modification to uprate R36 to a type W22 component.

Signed S. Mitsky.

(G. Mitchell)

Approved



WIRE WANTEST RSOZ

CREU WARNUS UNIT

LUCAS AEROSPACE LTD.
ELECTRICAL GROUP, BRADFORD ENGLAND
464

Report No. AED/ENV/480550
Figure Sheet No.

GAF 18789777

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APPENDIX B-4

VIBRATION TEST RESULTS

· EMI ELECTRONICS LIMITED, TEST HOUSE, FELTHAM

TEST REPORT No. ENV 2739 ETR 4605

TESTING AUTHORITY	DATE 25-6-80
E.M.I., ENVIRONMENTS DEPARTMENT D.G. of Q.A., APPROVAL NUMBER 10891	C.A.A. APPROVAL NUMBER AT/2925/49
TEST REQUESTED BY:	MANE: A.J.Littlewood Graviner Ltd., ADDRES: Colnbrook, SLOUGH.Berks.
TEST GLASSIFICATION:	Type approval
Custores order notes:	84808
CONTRACT NUMBER:	•
PROJECT:	249
B.M.I. REFERENCE MUNICIPAL	31401/38800
EQUIPMENT TENTED:	MAME: Computer Control Units Crew Warming Unit and SERIAL MOS: Single and Duel Detecto Heads DRAWING MOS:
TERE TO:	SPECIFICATION: See Report LIST:
CONCISSIONS:	
AUTHORITY AND REFERENCE:	
PREVIOUS SUBMISSIONS:	
REPORTED BY:	P.A.Brackley
APPROVED BT: 467	9Q.W
QUALITY OFFICER IN CHARGE, E.Q.D.	

SUBT 2 OF 13

Test. Gear used in conjunction with Report For ENV 2759

	722	eneral 10.	PLANT ID.
Withman			
Vibrator	Ling 805	201	1111/P
Ampilfier -	Ling HPA 8KV	158	111A/P
Oscillator	B & K 1025	338320	756/P
Voltmeter	B & K 2416	373223	800/P
Freq.Counter	Yenner	н9866	93/P
Auto Strobe	EMI A53	-	565/P
Oscilloscope	Telequipment D43R	5299	242G/P
	Amplifier A	• •	2425/P
	Amplifier A	-	242T/P
Charge Amplifier	Birchall CA-O1-2CH	38	2677/P
Stroboscope	EMI Type 6	_	582/P
Accelerometer	Bruel & Kjaer 4369	614776	. 502/ 5
Accelerometer	Endevce 224C	TC80	
Digital Randomise Control	Gen.Rad. TDV32PR	• ·	845/P
Teletype	Data Dynamics	-	845A/P
			·
•			
	468		-

1. INTRODUCTION

The following units were subjected to the following tests in accordance with the following specifications:

1.1 Crew Warning Unit

Crew Warning that Type 53813-202 Serial No.101 was subjected to a resonance search in accordance with Specification MIL-STD-810C; method 514.2-2:Procedure 1;Curve J of Fig.514.2-2 and to random vibration in accordance with Specification MIL-STD-810C: method 514.2; Procedure 1A;Figs.514-2-11A and 514-2-2A.

1.2 Computer Control Unit

The units, Computer Control Unit Type 53813-203, Serial No.100 (System A): Type 53813-204; Serial No.100 (System B) with Battery Card), were subjected to a resonance search in accordance with Specification NIL-STD-810C, Method 514.2.2; Procedure 1, curve J of Fig.514.2.2: to random vibration in accordance with Specification NIL-STD-810C, Method 515.2 Procedure 1A, Figs.515-2-11A and 514-2-2A, and to an acceleration test in accordance with Specification NIL-STD-810C, Method 513-2 Procedure 1.

. 1.3 Single and Dual Detector Heads

The unite, single detector head type 53521-012-and dual detector head type 53522-011, were both subjected to a resonance search in accordance with Specification MIL-STD-810C Method 514.2 Procedure 1, Curve G of Fig.514.2-2, and to random vibration in accordance with Specification MIL-STD-810C Method 514.2 Procedure 1A, Fig.514.2-11A and 514.2-2A.

2. TEST DETAILS

2.1 Crew Varning Unit

Resonance Search

The unit was subjected to a resonance search in each of the three mutually perpendicular axes at the following frequencies and levels:

5 - 14 Hs @ 0.10 peak-to-peak

14 - 23 Hs At 10

23 - 52 Hz @ 0.036 peak-to-peak

52 - 2000 Ha @ 5g

2.1 Crew Warning Wit (cont)

Random Vibration

The unit was subjected to random vibration at the levels shown in Fig.1 for one hour's duration in each of the three mutually perpendicular axes.

2.2 Computer Control Unit

Resonance Search

The units were subjected to a resonance search in each of the three sutually perpendicular axes at the following frequencies and levels:

5 - 14 Hs @ 0.10 peak-to-peak

14 - 25 Hz @ 1g

23 - 52 Hs @ 0.036" peak-to-peak

52 - 2000 Hs @ 5g

Random Vibration

The units were subjected to random vibration at the levels shown in Fig.1 for one hour's duration in each of the three sutually perpendicular axes.

Accleration

The units, System A and System B (with Battery Card), were subjected to a constant acceleration of 25.5g for 60 seconds in each direction of each of the three mutually perpendicular exes.

2.3 Single and Dual Detector Heads

Resonance Search

The units were subjected to a resonance search in each of the three sutually perpendicular axes at the following frequencies and levels:

5 - 14 Hm @ 0.10 peak-to-peak

14 - 23 Hs at 19

23 - 90 Hs @ 0.036" peak-to-peak

90 - 2000 Hz at 15g

Random Vibration

The units were subjected to random vibration at the levels shown in Fig.2 for one hour's duration in each of the three mutually perpendicular axes.

3. TEST RESULTS

3.1 Crew Warning Unit

Resonance Search

AXIS 1

A monitor accelerometer was mounted in positions A and B (see Fig.4)

Monitor Accelerometer position	Peak Resonance Frequency (Hz)	Input Level	Output Leve;
A	134	5	22
В .	142	5	37

AXIS 2

Between 115 Hs and 150 Hs, there was a resonance in the direction of the vibration, and between 150 Hs and 196 Hz there was a resonance normal to the direction of vibration.

AXIS 3

There was a resonance between 130 Hz and 234 Hz with a peak at 198 Hz.

Random Vibration

The unit was functionally tested by the visiting Graviner Engineer throughout the test. The unit functioned satisfactorily during the tests in Axes 2 and 3. After 35 minutes in Axis 1, the left-hand fire warning light failed to operate. The unit was opened by the visiting Engineer, and a broken lead was found at the soldered joint by the lamp. This was repaired and a tie rap was added to hold the cable and reduce movement. The test was then repeated and the unit found to function satisfactorily.

3.2 Computer Control Unit

Resonance Search - System A

Axis	Frequency	Comments
1 (normal to mounting face)	180-202 263	End board moving at bottom. Brown loom lead. (No resonance could be seen at the main cards)
2 (normal to long side)	73-94 94-112 112-118 140-162 162-300 255	Cards moving slightly together. Outside card moving more. Peak (especially outside cards) All cards moving, not together. All cards moving slightly Wire moving inside loom.
3 (normal to short side)	40-50 50-57 85-113 110 115-140 140-155 155 155-174 174-200	Slight movement of end card. All cards moving slightly. All cards moving slightly. Middle card moving. Single card moving strongly. Single card moving very strongly. Peak movement of single card. Single card moving strongly. Single card moving strongly.

Random Vibration - System A

The unit was functionally tested by the visiting Graviner Engineer throughout the test. The unit was found to function satisfactorily in all axes.

Acceleration - System A

The unit was functionally tested after each direction and axis before commencing with the following run. After the test was completed, the unit was returned to Graviners Ltd., when full functional tests were carried out. The visiting Engineer holds these functional test regults.

Sheet 7 of 13 REPORT NO: ENV 2739

Resonance Search - System B (without Dattery Card)

(

Axie	(Hs)	Comments
1	150-160	Outside board moving very slightly.
(normal	160-180	Inside and outside boards moving very slightly.
	180-200	Inside boards moving very slightly.
face)	208-230	End board moving.
2 (normal	93-118	Boards moving slightly together.
to long	118-123	Outside boards moving strongly. Other boards moving less strongly.
side)	123	Peak movement.
	123-160	Slight movement of boards.
	160-197	Very slight movement of boards.
3	48-53	End card moving slightly.
(normal	53-55	Hiddle and end cards moving slightly.
short	55-60	All cards moving slightly.
side)	75	Single card moving slightly.

Random Vibration - System B (without Battery Card)

The unit was functionally tested by the visiting Graviner Engineer throughout the test. The unit was found to function satisfactorily in all axes.

Sheet 8 of 13 REPORT NO: ENV 2739

Resonance Search - System B (without Battery Card)

Axia	Frequency (Hz)	Comments
1	150-190	Two support cards moving.
(normal	195	Battery and its support card moving slightly.
mounting	300 - 320	Support board moving.
face)	320	All long cards moving slightly.
	450-529	Front short board moving.
(norma)	65-109	Long cards moving together in the direction of vibration.
to long	109	Peak movement.
side)	135	Peak movement of outside card.
	140~200	All cards (except Battery Gard) moving.
	451	Outside card moving slightly. (No appreciable resonances could be seen of the Battery Card and its support card).
3	170-202	Short board moving.
(normal	202-214	Peak movement of short board.
short	270-340	Outside long card moving slightly.
side)	370-390	Short board moving slightly.

Random Vibration - System B (with Battery Card)

The unit was functionally tested by the visiting Graviner Engineer throughout the test. The unit was found to function satisfactorily in all axes.

Acceleration - System 8 (with Battery Card)

The unit was functionally tested after each direction and axis before commencing with the following run,

After the test was completed, the unit was returned to Graviners Ltd. where full functional tests were carried out.

The visiting Engineer holds these functional test results.

Sheet 9 of 13 REPORT NO: ENV 2739

3.3 Single and Dual Detactor number

Hesonance Search

In Axis 1 (see Fig.5), there was rocking on the mountings of the dual detector head between 368 and 385 Hx. There was no detectable resonances of the single detector head in this axis.

In Axis 2, the single head was rocking on its mountings, especially between 651 and 687Hz_{\odot}

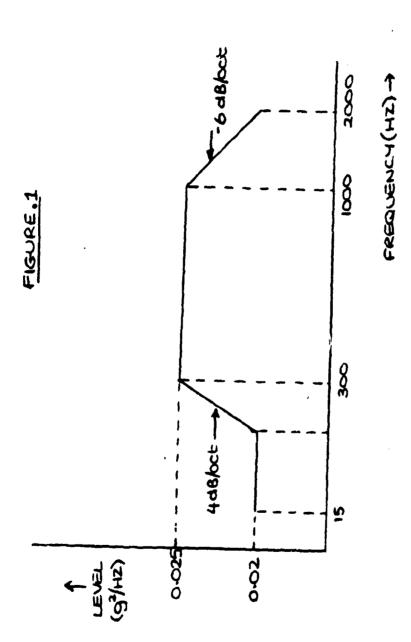
In Axis 3, the dual detector head was rocking on its sounts at 597 Hs.

Random Vibration

The units were functionally tested by the visiting Graviner Engineer throughout the test. Both units were found to function matisfactorily in all axes.

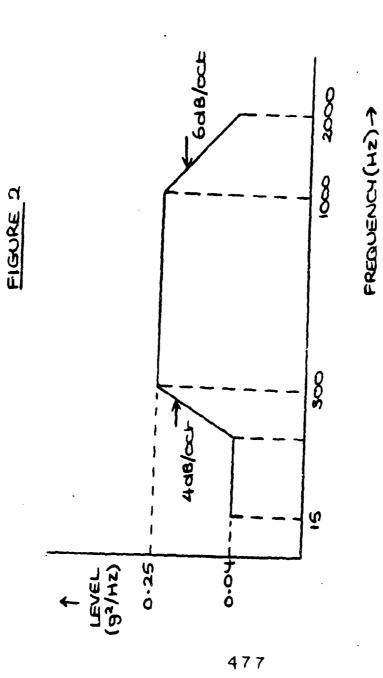
Reported by: P.A.Brackley Report No: ENV 2739 ETR 4605

Eupies to: Mr.R.Leney
Quality Service Department
Graviner Ltd.,
Colnbrook
SLOUGH.Bucks (4)

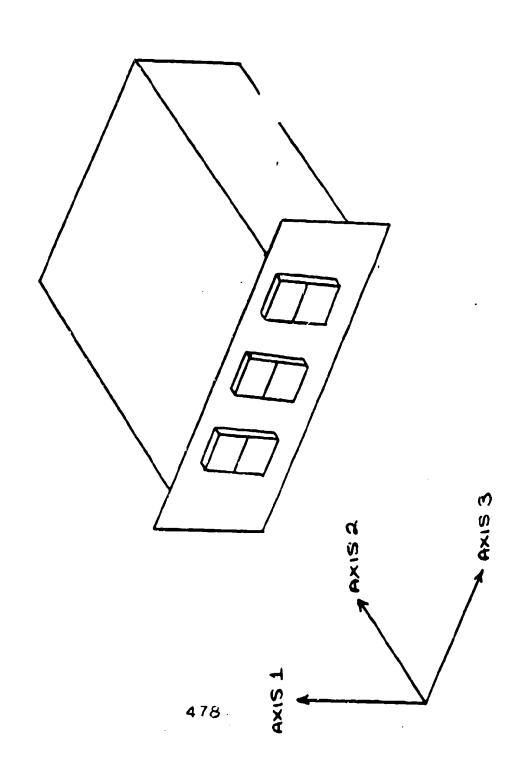


RANDOH VIBRATION LEVELS FOR CREW WARNING UNIT AND FOR COHPITER CONTROL UNITS.

4 76



SINGLE AND DUAL DETECTOR HEADS RANDOH VIBRATION LEVELS FOR



AXES OF CREW WARNING UNIT

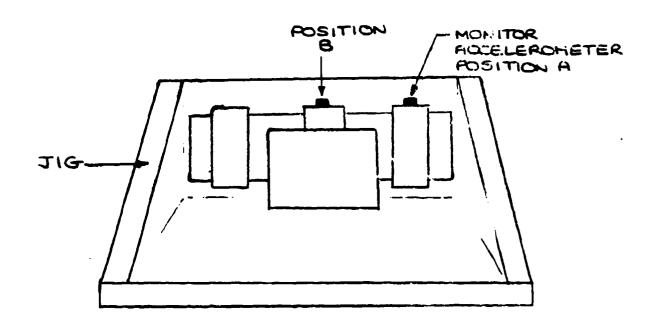
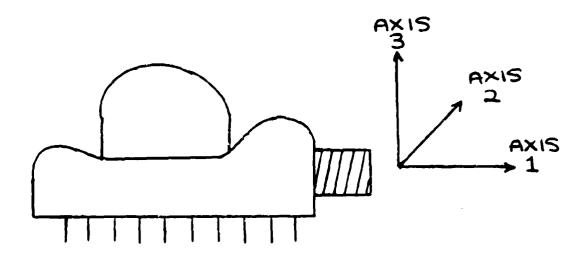


FIGURE 4 - POSITIONS OF HONITOR

ACCELEROHETER DURING THE RESONANCE

SEARCH FOR CREW WARNING UNIT



FIGURES - AXES OF SINGLE AND DUAL DETECTOR HEADS

British Acrospace DYNAMICS GROUP

HATFIELD, HERTFORDSHIRE ENGLAND

TEST HOUSE CERTIFICATE

A W 117
issued under Ministry of Defence Quality Assurance Board Approval No. 12718

Date 4 August 1980

To: Messrs Graviner Ltd. Contract No. IND 85604

Address Poyle Road, Colinbrook, Sub Contract Order No.

Slough, SL3 OHb Works Order No. AA 0942/00000

Environmental Engineering

LABORATORY

Report No. E T R 2297

Item Tested:— U-V Detector Head Type 53522-011 Serial Number XP 1 and XP7.

Type 53521-012 Serial Number XP1 and XP5

Test Specification:— MIL-STD-810, Nethod 515, Procedure 1, Category B.

Result Summary:— The four units were subjected to an acoustic environment to MIL-STD-810 for a duration of 30 minutes. The Overall Sound Pressure Level, measured using three Bruel & Kjaer Type 4135 microphones, was $154 \text{ dB re. } 2 \times 10^{-5} \text{ N/m}^2$.

Prepared by: (Sgd.) W.E. Teller (Printed) W.B. Betts

Certified that the tests have been carried out to the requirements of the Director-General of quality

Certified:

(Sed) W. B. Rous

for and on behalf of British Aerospace Dynamics Group

Distribution.
Customer
Customer's Chief Inspector
N U Q D
Chief Inspector. Hatfield

Head of Test House Laboratory

Hies

480

form No. 4844

APPENDIX R-5

TEST CERTIFICATE ETR 2297 ACOUSTIC VIBRATION

British Acrospace DYNAMICS GROUP

HATFIELD, HERTFORDSHIRE ENGLAND

TEST HOUSE CERTIFICATE

A W 117

issued under Ministry of Defence Quality Assurance Board Approval No. 12718

To: Messrs. Graviner 1td.

Contract No. IND 85604

Address Poyle Road, Colnbrook, Sub Contract Order No.

Slough, SL3 OHB Works Order No. AA 0942/00000

Environmental Engineering

LABORATORY

Report No. E T R 2297

item Tested:— U-V Detector Head Type 53522-011 Serial Number XP 4 and XP7.

Type 53521-012 Serial Number XP1 and XP5

Test Specification:— MIL-STD-810, Hethod 515, Procedure 1, Category B.

Result Summary.— The four units were subjected to an acoustic environment to MIL-STE-810 for a duration of 30 minutes. The Overall Sound Fressure Level, measured using three Bruel & Kjaer Type 4135 microphones, was $154 \text{ dB re. } 2 \times 10^{-5} \text{ N/m}^2$.

Prepared by: (Sgd.) WE Botts

Certified that the tests have been carried out to the requirements of the Director-General of quality

Certified:

(Sed.) W. B. Rolls

for and on behalf of British Aerospace Dynamics Group

Distribution.
Customer
Customer's Chief Inspector
N U Q D
Chief Inspector, Hatfield

Head of Test House Laboratory

.

483

form No. 4844

APPENDIX B-6

TABLES FOR APPENDIX B

Type: 53813-202.

SERIAL No. 100

TEST. STAGE: At 71°C

Q.5308	16.0 v. D.	c. INPUT.	29.0 v.D.C	INPUT.
No.	VOLTS.	m.A.	VOLTS.	m.A.
4.3.2.		77.3		105.0
4.3.3.		75.5		104.0
4.3.4.	/	57.2		81.0
4.3.5.		75.9		105.0
4.3.6.	1.7	8.5	1.4	15.0
4.3.7.	1.2	8.5	1.4	15.0
4.3.8	1.7	8.5	1.4	15.0
4.3.9.	1.7	8,5	1.4	15.0
4.6.0			N/A	
4.6.1.			N/A	
4.6.2.			N/A	
4.6.3.			N/A	
INSUL.	▶ 20 Meg			

Type: 53813-202.

SERIAL No. 101

TEST. STAGE: at -54°C

Q.5308	16.0 v. D.	c. Input.	29.0×D.C	INPUT.
No.	VOLTS.	m.A.	VOLTS.	m.A.
4.3.2.		73.0		105.0
4.3.3.		70.5		100.0
4.3.4.	'	71.0		100.0
4.3.5.		69.5		102.0
4.3.6.	1.7	7.9	1.5	15.0
4.3.7.	1.7	7.9	1,5	15.0
4.3.8	1.7	7.9	1.5	15.0
4.3.9.	1.7	7.9	1.5	15.0
4.6.0			N/A	
4.6.1.			N/A	
4.6.2.			N/A	
4.6.3.			N/A	
INSUL.	>20 Mag.		1	

U.V.A.F.D.S. COMPUTOR. CONTROL UNIT. SYSTEM 'A'

TYPE: 53813-203.

SERIAL No. 101

TABLE No. 3

SERIAL No. 101	7.
----------------	----

PARA No.	Q.5309		R	SULT	<u>. </u>			
4.1.	C	.29 OHA	15 .					
·	124	v. 4	120 Hz	A.C.	102v3	80 Hz.	16.0	v.⊅.c.
	MI.	MZ.	M3.	M4.	MI.	M2.	M3.	M4.
4. 2.1.			111	0.95			78	0.8
4. 2. 2.	110	112	68	0	85	89	34	0
4. 4.	95	101	56	0	75	80	30	0
4. 5.	111	118	228	0	97	91	134	
	102 v.	380Hz.	16.01	v. D.C .		1244	420K	A.C.
	SOE	(WLTS)	SIDE 2.	(VoLTS)	SIDA	(VOLTS)	SQE	(APTA)
	4.7.3.	5.44	4.7.4.	5,51	4.7.3.	5.45	4.7.4.	5.52
	4.7.5.	297	4.26.	296	4.7.4.	312	4.76.	310
4 8. 3.1.	2.	0.53	SECS.					
4.8.3.2.	t.	0.52	SACS.					
4.8.6.2.	SIDE 1.	0.337	SECS.	Sibe 2.	0.338	54	ಡ.	
4.8.6.3.	SIDE!	0.837	Secs.	SIDE 2.	0.169		iહ.	
4.8.9.	Size 1.	14.82	Secs	SIDE 2.	0.1675	54	ics.	
4.3.10.	SIDE 1.	14.82	SECS.	SIJE 2.	0.1676	S	دد. ا	
4.9. 2.		5.47	VOLTS.					
4.9.3.		4.39	Vo LTS.					
4.9.4.		14.9	VOLTS.					
4. 9. 5.		14.9	Vo US.					
4.10.2.	<u> </u>	27.6	Vo 475.					
4. 10.3.		27.6	Vo LTS					
4. 10.4.	L	27.8	V. LTS.					
4. 10.5.		27.8	Velts.					
4. 11. 3. 2.	11:	0.38	36cs.	داده	D.38	<u> </u>		· · · · · · · · · · · · · · · · · · ·
4. 11. 3. 2.	2.	0.38	SECS.	t.	D. 18	SECS.		
4.11, \$,5.	£2	1.9	SECS.					
4.11.6.	M4.	0.33	mA.					
4. 11. 7. 1.	GRUT	<u> </u>	v4					48
4.12.10.2.	t.	1.15	SECS.					
4.12.10.3.	16	0.82	SELS .					

U.V.A.F.D.S. COMPUTOR CONTROL UNIT SYSTEM'B' TYPE: 53813-204. SERIAL No. 101

WITHOUT BATTERY

TEST STAGE: at -54°C

PARA. No.		RE:	SULTS.			
4.1.	0.04	OHMS.				
	124v	420	H2. A.C.	102 v	380 Hz /	6.0.v.D.C.
	M2.	EM	M4.	M2.	M3.	M4.
4.2.1.		111	0.8		78	0.7
4.2.2	110	53	0	90	28	0
4.4.	99	50		78	28	
4.5,	116	220	0	90	135	n
			1251.	VOLTS		
	102	v 380Hz	1603.C.	124	v 420	Hz.A.C.
4. 7. 3.	5	.97			5,98	
4.7.4.	2	97			320	
4.8.3.1	E= 0	.52 SEC	<u>s</u>			
4.8.6.2	t. 0	.335 SEC	£			
4 8.6.3.	E. 0	. 168 SEC	4			
4.9.8.	E= 16	.77 SE	e s .			
4.8.9.	£. 0	.1675 \$84	S			_
4.4. 2.		.77 Ve	TS.			
4.9.3.	114	9 Vol	75.			
4./0.2.		67 Vo	US.			
4. 10.8.		N You	LTB.			
4. 10. 4.	27	.82 YoL	.75 .			
4. 10.5,	+		178.			
4.11. 3.2					A SEC	s <u>. </u>
4.14.6.	1.1.1.		<u>Ą. </u>			
4.11, 7,			4			
4.4.61			166 .		-	· - · - · · · · · · · · · · · · · · · ·
4.12.6.8	_		res			
APPENDIX	B. 4.7	y 6.	LTB . 4.	9	VOLTS.	

U.V.A.F.D.S. COMPUTOR. CONTROL UNIT. SYSTEM 'A'
Type: 53813-203. Test Stage: After Accolaration
SERIAL No. 100 TABLE NO. 5

PARA No.	Q. 5309		Ra	SULTS	<u> </u>			
4. 1.	0.0	MIO A						
	124	/. 4	20 Hz	A.C.	102v	380 Hz	16.0	v.D.C.
	M I.	MZ	M3.	M4.	MI.	MZ.	M3.	M4.
4. 2.1.			111	5.6			78	2,05
4. 2. 2.	106	115	68	0	73	90	34	0
4. 4.	96	101	58	0	73	90	31	0
4 . 5 .	110	120	225	0	8.8	94	137	0
	102 V.	380Hz.	16.01	1.⊅.c.		1244	420 M	A.C.
	SIDE	(WLTS)	SIDE 2.	(VOLTS)	SIDE!	(VOLTS)	SIDES	(MUS)
	4.7.3.	5.68	4.7.4.	5.62	47.3.	5.69	4.7.4.	5.53
	4.7.5.	294	4.7.6.	297	4.7.4.	313	4.76.	317
4 8. 3.1	٤٠	0.55	secs.					
4.9.3.2.	t	0.52	SECS.		·			 -
4.8.6.2.	SIDE 1.	0.38	SECS.	Side 2.	0.338		ieS.	
4.8.6.3.	SIDE 1.	0.168	Sta.	SIDE 2.	0.168		ics.	
4.8.9.	SIDE 1.	14.85	SECS.	SIDE 2.	14.A2		ICS.	
4.8.70.	SIDE 1.	0.1675	SECS.	SIDE 2.	0.167	5	<u>ادح.</u>	
4.9. 2.		5.71	VOLTS.				·	
4.9.3.		4.45	Vo LTS.					
4.9.4.	<u> </u>	114.9	VOLTS.	. 				
4. 9. 5.		114.9	VOLTS.					
4.10.2.		27.7	Vo LTS .					
4. <i>10-3</i> .		27.7	VOLTS.					 .
4. 10.4.	}	27.8	VALTS.				·	
4. 10.5.	<u> </u>		Nortz.					 -
4. // 3.4.	21:		SELS.	LL =	0.36	Eld.		
4. 11. 3. 3.	6.	0.38	SECS.	<u> </u>	0,38	SSES.		
4.11.3.5.	E:	2.3	SECS.					
4.11.6.	M4.		mA.					4
4. 11. 7. 1.	GAUT		/4.					
4.12.10.2.	F	1.16	Secs.					
4.12.10.3.	to	0 K'	SECS .					

TYPE: 53813-204. SERIAL No. 100 WITHOUT BATTERY

TEST STAGE: After Acceleration 9.5310

PARA. No.			SULTS.				
4. i.	0.015	<u> </u>	Hz. A.C.	/20.	200 //-	W	
	124v M2.			102 v 380 Hz 16.0 v 3.0			
	MA.	Ma	M4.	M2.	M3.	M4.	
4.2.1.		111	3.25		68	1.55	
4. 2.2.	1 20	60	<u> </u>	91	- x	<u> </u>	
4. 4.	106	51	0	80	29		
4.5.	121	226	1	95	136		
	10.2	v 380Hz	128 1. 1403 C	VOLTS		Hz.A.C.	
	102		1003.61			//L. // . C.	
4. 7.3.		5,63 297			320		
474.	tv (
4.8.3.1, 4.8.6.2							
4.0.6.3.							
	·						
4.0.8.	·		<u>es .</u>				
4.8.9. 4.9. 2.	<u> </u>	1.1675 S#4	78.				
4.9. 3.	!		:/:::				
4.10·2.			us.				
4.10.3.			L78.				
4. 10. 4.			.7s .				
4.10.5.			178 . 178 .				
4.11.3.2.				t 2. 0.	IA SEC		
4.11. 5. 2. 4.11. 6.		· · · · · · · · · · · · · · · · · · ·	···		1n 3#6	•	
4.11.7	GRUTI						
4.4.6.2			T:				
4.12.6.3.	T		res ,				
APPENDIX			75 4.		YOLTS.		

TYPE: 53813-202.

SERIAL No. 101

TEST. STAGE: After Acceleration

Q.5308 Para.	16.0 v. D.	c. Input.	29.0 v.D.C. INPUT.	
No.	Volts.	LTS. m.A.		m.A.
4.3.2.		72.5		100.0
4.3.3.		71.0		100.0
4.3.4.		79.5 •		110.0
4.3.5.		71.0		100.0
4.3.6.	1.7	7.95	1.5	14.5
4.3.7.	1.7	7.95	1.5	14.5
4.3.8	1.7	7.9	1.5	14.5
4.3.9.	1.7	7.95	1.5	14.5
4.6.0			N/A	
4.6.1.			N/A	
4.6.2.			N/A	
4.6.3.			N/A	
INSUL.	> 20 Meg.		1	

TABLE NO.8

Detector Type 53522-011, S/No. XP6 and Detector Type 53521-012 S/No.ENV.

After Acceleration

Calibration Count 75 p.p.s.

Detector Unit Type	5 3 5 2 2	-011	53521-012
	XP	6	ENV
	A	В	
Q.5304 Para.			
5.2	76.0	77.4	97.0
5.2.1.	28.0	30.0	34.0
5.3.	0	0	0
5.4.1.	SATIS	FACTORY	SATISFACTORY
5.4.2.	SATISFACTORY		SATISFACTORY
5.5	>20 Me	gohms	>20 Megohms
•	1		

TYPE: 53813-202.

Ç.

SERIAL No. 101

TEST. STAGE: After Resonance Search

Q 5308 PARA.	16.0 v. D.	c. Input.	29.0 v.D.C	INPUT.
No.	Volts.	m.A.	VOLTS.	m.A.
4.3.2.		71.0		100.0
4.3.3.		70.0		100.0
4.3.4.		71.0		100.0
4.3.5.		69.5		100.0
4.3.6.	1.7	7.9	1.4	14.5
4.3.7.	1.7	7.9	1.5	14.0
4.3.8	1.7	7.9	1.5	14.0
4.3.9.	1.7	8.0	1.5	14.0
4.6.0			N/A	
4.6.1.			N/A	
4.6.2.			N/A	
4.6.3.			N/A	
INSUL.	>20 Meg.		1	

TYPE: 53813-202.

SERIAL No. 101

TEST. STAGE: During Random Vibration - Plane 1.

Q5308 PARA.	16.0 v. D.	C. INPUT.	29.0 x.D.C. INPUT.		
No.	Volts.	m.A.	VOLTS.	m.A.	
4.3.2.		71.0		100.0	
4.3.3.		66.0		100.3	
4.3.4.		70.0		100.0	
4.3.5.		69.0		100.0	
4.3.6.	1.7	8.0	1.5	15.0	
4.3.7.	1.7	8.0	1.5	15.0	
4.3.8	1.7	8.0	1.5	15.0	
4.3.9.	1.7	8.0	1.5	15.0	
4.6.0			N/A		
4.6.1.			N/A		
4.6.2.			N/A		
4.6.3.			N/A		
INSUL.	> 20 Meg.				

TYPE: 53813-202.

SERIAL No. 101

TEST. STAGE: During Random Vibration - Plane 2.

Q.5308 PARA.	16.0 v. D.	C. INPUT.	29.0 x D.C	INPUT.
No.	Volts.	m.A.	VOLTS.	m.A.
4.3.2.		70.0		100.0
4.3.3.		49.0		95.0
4.3.4.		52.0		100.0
4.3.5.		67.0		100.0
4.3.6.	1.4	8.0	1.5	15.0
4.3.7.	1.7	8.0	1.5	15.0
4.3.8	1.7	8.0	1.5	15.0
4.3.9.	1.7	8.0	1.5	15.0
4.6.0			N/A	
4.6.1.			N/A	
4.6.2.			N/A	
4.6.3.			N/A	
INSUL.	> 20 Meg.			

TYPE: 53813-202.

SERIAL No. 101

TEST. STAGE: During Random Vibration - Plane 3.

9.5308 PARA.	16.0 v. D.	C. INPUT.	29.0 v.D.C. INPUT.		
No.	Volts.	m.A.	VOLTS.	m.A.	
4.3.2.		69.0		100.0	
4.3.3.		66.0		98.0	
4.3.4.		69.0		100.0	
4.3.5.		68.0		99.0	
4.3.6.	1.7	7.9	1.5	14.5	
4.3.7.	1.7	7.9	1.5	- 14.5	
4.3.8	1.7	7.9	1.5	14.5	
4.3.9.	1.7	7.9	1.5	14.5	
4.6.0			N/A		
4.6.1.			N/A		
4.6.2.			N/A		
4.6.3.			N/A		
INSUL.	> 20 Heg.				

TYPE: 53813-202.

SERIAL No. 101

TEST. STAGE: After Vibration Testing.

Q.5308	16.0 v. D.	b·ov. D.C. INPUT.		.INPUT.
No.	VOLTS.	m.A.	VOLTS.	m.A.
4.3.2.		73.0		100.0
4.3.3.		72.0		100.0
4.3.4.		80.0		110.0
4.3.5.		71.0		100.0
4.3.6.	1.7	8.1	1.5	14.5
4.3.7.	1.7	8.1	1.5	14.2
4.3.8	1.7	8.1	1.5	14.2
4.3.9.	1.7	8.1	1.5	14.0
4.6.0			N/A	
4.6.1.			N/A	
4.6.2.			N/A	
4.6.3.			N/A	
INSUL.	> 20 Meg.		1	

System A. C.C.U. Type 53813-203 S/No.100

Testing during random vibration was limited to response and reset time tests.

	Response Time	Reset Time
Plane 3	1.18 seconds	0.876 second
	1.30 seconds	0.931 second
	1.15 seconds	0.902 second
Plane 2	1.30 seconds	0.936 second
	1.20 seconds	0.885 second
	1.18 seconds	0.984 second
Plane 1	1.16 seconds	0:90 second
	1.25 seconds	0.98 second
	1.26 seconds	0.93 second

U.V.A.F.D.S. COMPUTOR. CONTROL UNIT. SYSTEM 'A' TYPE:53813-203. TEST STAGE: After Vibration Test

TEST STAGE: After Vibration Testing

SERIAL No. 100 TABLE NO. 15

Para No.	Q.5309		RE	SULTS				
4.1.	0.16	OHA	AS.		_			
	124	v. 4	120 Hz	A.C.	102 × 380 Hz 16 OV. D.C.			v.D.C.
	MI.	M2.	M3.	M4.	MI.	M2.	M3.	M4.
4. 2.1.			111	5.1			76	2.1
4. 2. 2.	109	117	63	0	85	92	33 -	0
4. 4.	9.7	102	56	n	75	80	30	0
4. <i>5</i> .	111	118	222		. 88	105	135	0
	102 x	380Hz.			/	244	420 M	A.C.
	SIDE	(WLTS)	SIDE 2.	(APT12)	SIDE!	VOLTS)	Sibe 2	(AMZ)
	4.7.3.	5.65	4.7.4.	5.49	47.3.	5.55	4.7.4.	5.49
	4.7.5.	295	4.76.	297	4.7.4.	312	4.76.	315
4 2. 3.1.	٠	0.55	secs .					
4.8.3.2.	t.	0.54	SECS.					
4.8.6.2.	SIDE 1.	0.337R	Ecs.	S.34 2.	<u>n.</u>	3378 56	<u>ಡ.</u>	<u>-</u>
4.8.6.3.	SIDE!	0.1683	SECS.	SIDE 2.	٥.	1683 S 1	KS.	
4.8.9.	SIDE 1.	14.84	S 6 CS.	SIDE 2.	14.	R2 S6	ıcs.	
4.2.10.	SIDE!	0.1676	SECS.	SIJE 2.	<u>o.</u>	1676 \$	<u>ાડ.</u>	
4.9. 2.		5.48	OLTS.					
4.9.3.		4.42	Vo LTS.					
4.9.4.	<u></u>	15.0	VOLTS.					
4. 9. 5.	L '	ره. دا.	VO LTS.	- 				
4. 10 - 2.		27.6	VOLTS.					
4. 10-3.		27.6	VOLTS.					
4. 10.4.	├ —		VOLTS.					
4. 10.5.	-		Vo LJS .					
4. 11. 3. 2.	11:		Secs.	cr.	0.11	SECS.		
4.11.3.3.	5.		SECS.	<u>t•</u>	0.30	SECS.		
4.11.3.5.	E:		SECS.					
4.11.6.	M4.		mA.					
4. 11. 7. 1.	GRUT	1.2	/4.					50
4.:2.10.2.	6.		SECS.					
4.12.10.3.	<u>L</u>	0.2	SECS.					

System B, C.C.U. Type 53813-204 S/No.100 Without Battery Card

Testing during random vibration was limited to response and reset times.

	Response Time	Reset Time		
Plane 3	0.964 second	0.955 second		
Trunc 3	1.09 seconds	0.845 second		
	0.964 second	0.905 second		
Plane 2	1.02 seconds	0.903 second		
	0.938 second	0.957 second		
	0.775 second	0.898 second		
Plane 1	0.857 second	0.933 second		
	0.885 second	0.839 second		
	0.932 second	0.915 second		

U.V.A.F.D.S. COMPUTOR CONTROL UNIT SYSTEM'B' TYPE: 53813-204. SERIAL No. WITHOUT BATTERY.

TEST STAGE: After Vibration Testing Q.5310

ARA. No.		R E	SULTS.			
4.1.		OHMS.				
	124v	420	Hz. A.C.	102 V	380 Hz .	6.0vD.C.
	M2.	Ma	M4.	MZ.	M3.	M4.
4.2.1.		1 88	3, 3		60	1.6
4. 2.2.	: 19	60	0	100	10	0
4.4.	108	51	0	83	28	
4.5.	120	192	^	95	119	0
			51751.	VOLTS		
	102	v 380 Hz	16.03.C.	124	v 420	Hz.A.C.
4 . 7. 3.		5.6			5.	
4.7.4.		296		<u> </u>	319	
4.8.3.1.		.49 SEC				
		. 135 SE 6	نة.			
48.6.3.	h	168 SE				
4.8.8.			<u>65</u>			
4.8. 9.	E ? 0.	1677 \$86				
4.9. 2.	\———		LTS.			
4.9.3.	114.		L75.			
4./0.2.	27.		Us.			
4. 10.3.	27.		LTE.			
4. 10. 4.			L78 .			
4. 10.5.			176.	.		
4.11. 3. 2.				EL. 0.38	586	<u>s.</u>
4.11.6.			<u> </u>			
4.11.7.	GRUTI		<u>4.</u>			5
4.12.6.3.	·	<u></u>	[6 6 . [6 6 .			
PPENDIX			LTs . 4.		VOLTS.	

System B. C.C.U. Type 53813-204 S/No.100 With Battery Card

Testing during random vibration was limited to response and reset times.

	Response Time	Reset Time
Plane 3	0.940 second	0.953 second
•	1.08 seconds	0.907 second
	0.996 second	0.926 second
Plane 2	1.06 seconds	0.627 se cond
	0.858 second	0.661 second
	0.924 second	0.889 second
Plane I	0.952 second	0.620 second
	1.100 seconds	0.921 second
	0.911 second	0.971 second

TYPE: 53813-204. SERIAL No. 100

WITHOUT BATTERY

TEST STAGE: After libration leveling

. No.		RES	SULTS.			
	0.04	OHMS.				
	124v	420	Hz. A.C.	102 v	3BQHz /	GOVD.C.
	Ma.	EM	M4.	MZ.	мз.	M4.
2. /. [90	3,4		60	1.8
2.2	120	58	n	102	30	n
٠. [106	50	n	94	28	0
5.	121	213	n	108	130	n
			IDE 1.	VOLTS	<u>.</u>	
	102	v 380Hz	16.03.C.	124	v 420	Hz. A.C.
. j.		5.6		L	5.61	
7. 4.		297.1			318,2	
B. 3. 1.	t *	0.48 58C	s <u>. </u>		-	
3. 6.2.	t:	1.3% SEC	s <u>. </u>			
1. 6. 3.	r.	7, 168 5#C	.s			
B. 8 ,	t. 1	4.77 580	<u> </u>			·
3. 9.	£:	0.1675 \$86	<u>s</u>			
9. 2.	 	4.35 VOL	75,			
7. 3.		4.41 VOL	TE			
0.2.		7.59 Vo	Js.			
/o . 3 .	<u></u>	7.59 Ya	LTs.			
0.4.	2	7.59 YOL	.TS .			
10.5.		7.59 Vo	L78.			
11. 3. 2.	<u> </u>	0.18 SE	ES	ċ₽• ∩. 3K	SEC	S .
11.6.	M4.	3.4 M			<u> </u>	
.11, 7.	GRUTI		4			
12.6.2.	<u> </u>		<u> </u>			
12.6.3.	15.	0.67 \$1	res.			

TABLE NO. 20

Detector Unit Type 53522-011 S/No.XP6 and Detector Type 53521-012 S/No. ENV.

Testing during random vibration was limited to response and reset times.

	53522-011 (2	XP6)	53521-012 (ENV)			
	Response Time	Reset Time	. Response Time	Reset Time		
Plane 3	0.903 second	0.942 sec.	1.06 seconds	0.895 sec.		
	0.847 second	0.947 sec.	0.790 second	0.953 sec.		
	1.20 seconds	0.975 sec.	1.16 seconds	0.931 sec.		
Plane 2	1.19 seconds	0.963 sec.	0.929 second	0.631 sec.		
	0.968 second	0.949 sec.	1.03 seconds	0.979 sec.		
	1.2 seconds	1.13 sec.	0.996 second	0.931 sec.		
Plane I	1.03 seconds	0.989 sec.	1.08 seconds	0.928 sec.		
	i.17 seconds	0.839 sec.	1.09 seconds	0.878 sec.		
	0.770 second	0.870 sec.	0.934 second	0.870 sec.		

After Vibration testing. Calibration count 64.5 p.p.s.

	53522-01	1 (XIP6)	53521-012(ENV)	
	A	В		
5304 ara. 5.2.	66.74	69.79	90.51	
.2.1.	33.1	28.0	41.6	
5.5.	20 Megon	im's	>20 Megohms	

TABLE NO.21

Detectors Type 53522-011, S/Nos. XPI and XP7 and Detectors Type 53521-012, S/Nos. XPI and XP5.

Before acoustic vibration. Calibration count 52 p.p.s.

	5 35	22-01	<u> </u>	53521-0	012
XPI XP7		XIP I	XP5		
A	3	A	В		
79	65	54	73	68	58
46	28	25	29	36	56
0	0	0	0	o	o
5	ATISF	ACTORY	1	SATI	SFACTORY
SATISFACTORY				SATI	SFACTORY
>20 Megohms				>20 Me	goh ns
	79 46 0	XP1 A 3 79 65 46 28 0 0 SATISE SATISE	XP1 XP2 A X A 79 65 54 46 28 25 0 0 0 SATISFACTORY SATISFACTORY	A A B 79 65 54 73 46 28 25 29 0 0 0 0 SATISFACTORY SATISFACTORY	XP1 XP7 XP1 A B 3 A B 79 65 54 73 68 46 28 25 29 36 0 0 0 0 0 SATISFACTORY SATIS SATISFACTORY SATISFACTORY

After acoustic vibration. Calibration count 59 p.p.s.

Detector Type	53522-011				5 3 5 2 1 -	012	:
	XI	'1	XIP 7		XP I	XP5	
Q.5304 Para.	Α	В	A	В			
5.2.	76	63	49	70	70	55	:
5.2.1.	: 40	28	32	31	35	24	
5.3.	0	0	0	0	0	o	:
5.4.1.	1	SATIS	FACTORY	, (SATI	SFACTORY	•
5.4.2.	SATISFACTORY				SATISFACTORY		
5.5	>	0 Meg	ohms		>20 N	le gohma	

TYPE: 53813-202.

SERIAL No. 101

TEST. STAGE: After Shock Testing

Q.5308 PARA.	16.0 v. D.	C. INPUT.	29.0 v.D.C. INPUT.		
No.	Volts.	m.A.	VOLTS.	m.A.	
4.3.2.		71/20		100.0	
4.3.3.		70.5		100.0	
4.3.4.		78.5		110.0	
4.3.5.		69.5		100.0	
4.3.6.	1.7	7.8	1.5	14.5	
4.3.7.	1.7	7.8	1.5	14.5	
4.3.8	1.7	7.8	1.5	14.3	
4.3.9.	1.7	7.8	1.5	14.3	
4.6.0			N/A		
4.6.1.			N/A		
4.6.2.			N/A		
4.6.3.			N/A		
INSUL.	> 20 Meg.				

U.V.A.F.D.S. COMPUTOR. CONTROL UNIT. SYSTEM 'A'

TYPE: 53813-203.

SERIAL No. 100

TABLE NO. 23 TABLE NO.23

Para No.	Q.5309		RE	SULT	<u>. </u>			
4.1.	0.07 OHMS.							
	124	124v. 420Hz A.C.			102 × 380 Hz 16 0 v.D.C.			
1	MI.	M2.	M3.	M4.	MI	MI.	M3.	M4.
4. 2.1.			110	5.3			75	2.1
4. 2. 2.	110	115	48	0	85	100	35	n
4	95	100	54	0	75	78	30	0
4 . 5 .	110	120	220	n	.96	95	1 36	0
	102 v.	380Hz.		1.⊅.c .		1244	420 K	
	SIDE	(WLTS)	SIDE 2.	(A0T12)	SDE!	(VOLTS)	Si)82	(APTA)
	4.7.3.	5.69	4.7.4.	294	47.3.	5.7	4.7.4.	314
	4.7.5.	5.53	4.76.	297	4.7.4.	5.53	4.76.	317
4 8. 3.1.	t•	0.56	Secs .					
4.8.3.2.	<u> </u>		Sees .					
4.8.6.2.	Side 1.	0.337	SECS.	5,342.	0.)?* SI	ಡ.	
4.8.6.3.	Sibel.	0.173	SECS.	SIDE 2.	n,	173 St	ics.	
4.8.9.	Side 1.	14.82	SECS.	5138 2.	14.	m. Si	ics.	
4.2.10.	SIEE!		SECS.	SI3 8 2.	0,	172 \$	<u>ائ.</u>	
4.9. 2.		5,34 1	OLTS.					
4.9.3.		4.51	Ve LTS.			·		·
4.9.4.			VOLTS.					
4, 9.5.			Vo LTS.					 -
4.10.2.		:1.1	VOLTE.					
4. 10.3.		27.7	VOLYS.					 -
4. 10.4.			VA LTS.			 		
4. 10.5.	<u> </u>		VOLTS.					 .
4. 11. 3. 2.		0.18 0.18	Secs.		0,38	Eles.		
4.11.3.3.	<u>.</u>		SECS.	<u> </u>	Л. ЗН	. इ.स		
4.11.3.5.	M4.		SECS.					
4.11.6.	GAUT		mA . /4					
4.12. 2. 2.	L	1,15	Sacs.					5
4.12.16.3.	-	0,68	SECS.					

TABLE 10.24

TYPE: 53813-204. SERIAL No. 100

et State ...

TEST STAGE: After Shock Testing
Q.5310

ARA. No.			SULTS.						
4.1.	0.03	Onno.							
	1244	420 Hz. A.C.		102 v 380 Hz . 16.0 v D.C					
	M2.	EM	M4.	M2.	мз.	M4.			
4.2.1.		86	5,6		60	2.0			
4. 2.2	120	55	0	90	28	n			
4.4.	105	48		80	25	<u> </u>			
4.5.	128	187	0	95	112	0			
	SIDE 1. VOLTS.								
	102 v 380Hz 16.03.C.			1244 420 Hz. A.C.					
4. 7. 3.	5.68			5,40					
4.7.4.	296			321					
4.8.3.1.	₹ 0.	.48 SEC	s						
4.8.6.2	t: 0.	. 136 SEC	s		·				
4.8.4.3.	t. 0	. 173 SEC	s						
4.8.8.	C= 14	Sac	:S .						
4.8.9.	t = 0.	. 172 SEC	s .						
4.9. 2.	4.	4 VOL	75.						
4.9.3.	1	15 YOL	75.						
4./0.2.	27	.7 Yo l	Is.						
4. 10.3.	27	R Yel	Js.						
4. 10. 4.	27.	9 YOL	TS .						
4. 10.5.	27	.9 Yo .	LTS .						
4.11. 3. 2.	८\$= ∩.	.18 SE	ES.		SEC	£ .			
4.11.6.	M4. 3.	.8 m	Α						
4.11.7.	GRUTH	L. V4	4.						
4.12.6.1.	٠ · •	#1 58	ζ Ś .						
4.12.6.3.	Z. n.	SE SE	'cs.						

Detector Unit Type 53522-011 S/No. XP6 and Detector Unit Type 53521-012 S/No. ENV

Response and Reset times after shock testing.

53522-011(XP6)	53521-012(ENV)		
Response Time	Reset Time	Response Time	Reset Time	
1.28 sec.	1.01 sec.	0.958 sec.	0.825 sec.	
1.28 sec.	1.00 sec.	0.782 sec.	0.94 sec.	
1.28 sec.	0.82 sec.	0.992 sec.	0.60 sec.	